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Recent achievements and pending challenges in Gallium Nitride vertical device development

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Abstract

A brief overview of the latest achievements in Vertical GaN device technology is presented here, underlining the key issues that were overcome in the last decade. The remaining challenges are discussed for each device type.

1. Introduction

GaN technology is an ever-expanding topic of research and development, proving its potential to solve several challenges in power conversion that cannot be addressed by Si. For instance, medium voltage (650-900V) devices using the HEMT configuration [1] have been able to reduce form factor at the system level by driving circuits at higher frequencies (100KhZ-1Mhz) and eliminating heat sinks or reducing cooling requirements. This alone sparked the interest in GaN research to save space, energy and ultimately cost of power conversion. However, in power conversion the demand of high current from a single chip for a rated voltage is a standard need. Particularly when the market is favorable towards electrification of cars and other means of transportations, GaN must expand its scope to provide high power solutions with higher power density compared to Si, and even SiC. Vertical devices have been the choice of power device engineers for economic use of the material and maximum use of its physical properties (which allow highest possible blocking field, field mobility, etc.). GaN vertical devices [2-11], therefore, carry all the advantages offered by vertical geometry and are being explored increasingly with emphasis on material and device needs.

2. Results and Discussion

In this work, we will go over the three types of vertical devices for power conversion that we are pursuing in our group and go over the achievements and challenges in each.

Current Aperture Vertical Electron Transistors (CAVETs)

CAVETs [2,3] were the first vertical devices that demonstrated the potential of GaN vertical devices. CAVETs are realized with Mg-ion implanted current blocking layers (CBLs) with regrown channel (Figure 1(a)). Alternatively they can have Mg-doped CBLs with a regrown channel layer on a trench. We have explored either way of realizing CAVETs with successful results and challenges around obtaining an effective CBL. Recently with p-GaN gating structure, over 450V was achieved with a CAVET with its channel was regrown using ammonia Molecular Beam Epitaxy (MBE)[7]. Devices showed no dispersion at 5µs pulse widths (see Figure 3(a)). The p-GaN gated CAVET showed

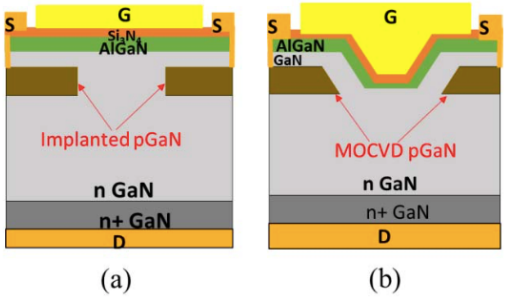

Figure 1. (a) CAVET with implanted [Mg]-GaN as CBLs. (b) Trench CAVET with MOCVD p-GaN as CBLs.

a significant improvement over current state-of-art AlGaN/GaN CAVETs with ion-implanted CBL [2], both in terms of increased breakdown voltage of over 500V, as well as reduced off-state leakage at a given bias. However, two key issues that are yet to be addressed are the out diffusion of implanted [Mg] during high-temperature regrowth process and the difficulty in achieving normally OFF operation. In a parallel study [8] we explored an all-MOCVD based CAVET with Mg-doped CBL. In this paper, a trench CAVET based on a bulk GaN substrate was designed and fabricated using a metal organic chemical vapor deposition (MOCVD) regrown channel and aperture. The schematic of the trench CAVET is shown in Fig. 1(b). Instead of using Mg-implanted p-GaN for the CBL, the trench CAVET adopts MOCVD-grown Mg-doped p-GaN as the CBL material.

The buried Mg-doped p-GaN CBL was activated successfully implementing a post-MOCVD regrowth annealing process. The buried p-n body diode sustained remarkably a high breakdown electric field of 3.8 MV/cm. The maximum saturation current was limited to 62 A/cm^2, due to high source contact resistance as a consequence of low source metal annealing temperature (600 °C), as well as Mg-incorporation into the regrown AlGaN/GaN sidewall. The transistor breakdown voltage of 225 V was limited by gate to drain leakage

The source-to-drain body diode offering a reverse characteristic blocking up to 1 kV, demonstrated a blocking electric field of 3.8 MV/cm. This is as high as the theoretical breakdown field of GaN.

Static Induction Transistors (SITs)

The concept of Static induction transistor (SIT) was introduced by Nishizawa and in 1975, experimental SITs were fabricated and the drain current of this device was shown to follow the predicted space-charge injection mode.

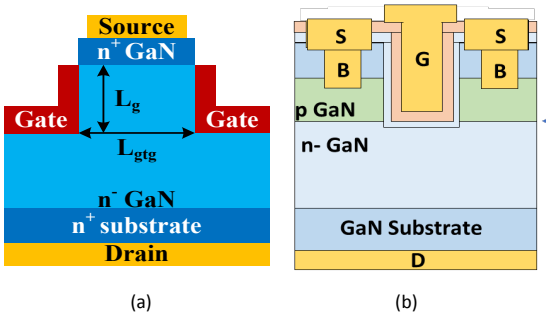

Figure 2. Schematic of (a) SIT without any need for p-type GaN (b) OG-FET with in situ oxide and regrown GaN interlayer

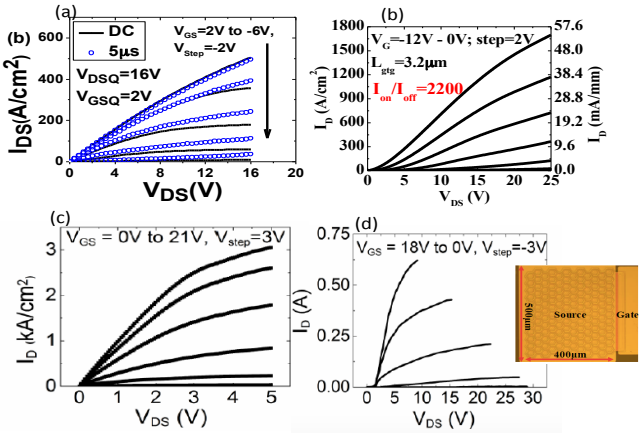

Figure 3. Drain Characteristics of (a) CAVET overlaid with its pulsed I-V characteristics (b) SIT showing triode-like behavior (c) OG-FET unit device and (d) scaled OG-FET

A typical recessed gate SIT structure with bottom and sidewall contacts was shown in Fig. 2(a). SIT is a class of short-channel Field Effect Transistors. The current, which flows vertically between the source and the drain, is controlled by electrostatic potential barrier induced by the two opposed gates. Thus, SIT shows a triode-like unsaturated output characteristics (see Fig. 3(b)). SiC SITs have shown the potential for high power and high frequency applications. With higher electron mobility and higher saturation velocity than SiC, GaN SITs have the potential to operate at higher frequency with higher output power. In our work, we successfully designed and fabricated the GaN SIT using self-aligned process [9].

Oxide Gated-FET (OG-FET) or MOSFETs

To date, most successful results have come out of MOSFETs. MOSFETs with an un-doped GaN interlayer as a channel and in-situ MOCVD oxide, called OG-FET (Fig. 2 (b)), reported by Gupta et al. have demonstrated superior performance with low specific on-state resistance (R_{on}) [10]. We have successfully performed device scaling of the OG-FET to realize high output current as shown in Figure 3(c-d) [11].

OG-FETs have shown promising blocking voltages for high power performance. During the presentation we will share our latest data showing >1KV blocking voltage with R_{on}<3mΩcm^2.

Although CAVETs look promising in the mid-voltage range (600V-1KV) offering high frequency operation (due to the 2DEG formed by AlGaN/GaN), it relies on robustness of the buried p-n junction. SIT on the other hand alleviates the need of any p-type GaN but required very tight scaling to realize good pinch-off characteristics.

While OG-FETs have shown promising performance, they are plagued by the limitation imposed by the buried p-n junction.

In this presentation we will also go over the challenges faced by each of these device types and discuss paths to overcome those.

3. Conclusions

Three types of vertical GaN devices are presented and their latest results together with their pending challenges are discussed.

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