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Demonstration of Reduction in $V_{ce(sat)}$ of IGBT based on a 3D Scaling Principle

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Abstract

A three-dimensional scaling principle for the collector-emitter saturation voltage, $V_{ce(sat)}$, reduction in IGBTs has been proposed. A significant reduction in the $V_{ce(sat)}$ from 1.70 to 1.26 V has been experimentally confirmed by the 3D scaling from k=1 to k=3.

1. Introduction

Performance improvements in Si-based insulated gate bipolar transistors (IGBTs) are attractive for the implementation to large lower-price markets [1]. Lowering of the collector-emitter saturation voltage, $V_{ce(sat)}$, is an essential requirement to suppress the energy loss for IGBTs. To meet the requirement, a structural design based on injection enhancement (IE) to increase the electron injection as well as hole injection and accumulation in the n-base region has been utilized so far [2-4]. A recent simulation study based on 2D scaling in trench gate IGBT shows significant $V_{ce(sat)}$ reduction by scaling the structures and the operation voltage as well [5]. The purpose of the presentation is to experimentally demonstrate the $V_{ce(sat)}$ reduction with a 3D scaling principle by fabricating IGBTs for both k=1 and 3 generations [6]. The 3D scaling scheme has been built to ease the fabrication processes and by adding a scaling concept along the perpendicular dimension to the cross-section to avoid latch-up free operations.

2. Proposal of a 3D Scaling Principal

The basic structure of a trench gate IGBT is shown in figure 1. As the concept of the scaling is based on enhancing the IE effect, the mesa width (S), the gate length (L_g) and the oxide thickness of the MOSFET (t_{ox}) were scaled by a factor of $1/k$. A shorter cell pitch (W) results in the loss of the IE effect, and longer W leads to larger area decreasing the current density. Therefore, the W is kept to be 16 µm from simulation study, as shown in figure 2. Although the IE effect may weaken to some extent, trench depth (D_T) is decreased by a factor of $1/k$ to avoid the narrow mesa problems [7] and to ease the manufacturability. Also, the trench width (W_T) is scaled moderately with a factor of $2/k$ as the parameter basically does not affect the performance. Instead, wider trenches contribute to the reduction in parasitic resistances of gate electrodes. Scaling in the shallower p-base region may cause latch-up, therefore, length of emitter (L_{n+})/body (L_{p+}) periodic patterns were also scaled by a factor of $1/k$. The scaling in operation voltage results in the reduction of switching energy by $1/k^2$, and the voltage has better compatibility with the integration of CMOS logic circuits. The feature sizes of the fabricated devices are listed in table I.

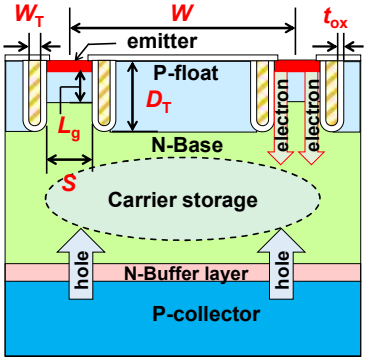

Figure 1 Structural parameters of a trench gate IGBT.

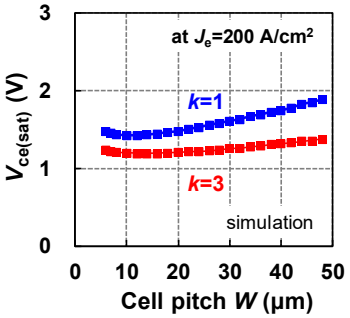

Figure 2 Simulation study shows optimum W for $V_{CE(sat)}$ reduction. A W of 16 µm is adopted in this work.

Table I Feature sizes based on the 3D scaling principle.

Parameters in IGBT, symbols	k=1	k=3	Scaling factor
Cell pitch, W (µm)	16	16	1
Mesa width, S (µm)	3	1	$1/k$
Trench depth, D_T (µm)	6	2	$1/k$
Trench width, W_T (µm)	1.5	1.0	$2/k$
P-Base depth, D_P (µm)	3	1	$1/k$
N-Emitter depth, D_N (µm)	0.4	0.13	$1/k$
Gate oxide thickness, t_{ox} (nm)	100	33	$1/k$
Length of p^+ region, L_{p+} (µm)	4.5	1.5	$1/k$
Length of n^+ region, L_{n+} (µm)	4.5	1.5	$1/k$
Gate voltage, V_g (V)	15	5	$1/k$

3. Device Characteristics

Emitter current densities on collector voltage (J_e-V_{ce}) as a function of V_g are shown in figure 3 and 4 for k=1 and 3, respectively. It is confirmed that the J_e slope in the low-V_{ce} linear region is much steeper for the k=3 case, suggesting the reduction in the on-resistance. Moreover, it was confirmed that $V_{ce(sat)}$ (defined at J_e=200 A/cm^2) significantly reduced from 1.70 V (k=1) to 1.26 V (k=3), by the proposed scaling.

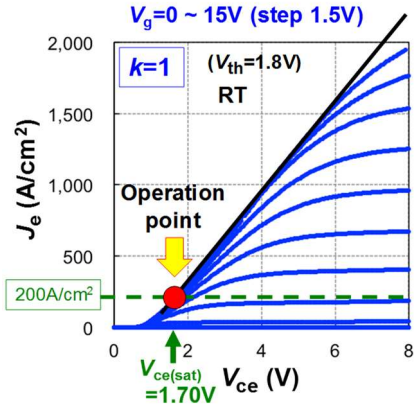

Figure 3 J_e-V_{ce} characteristics of an IGBT with k=1.

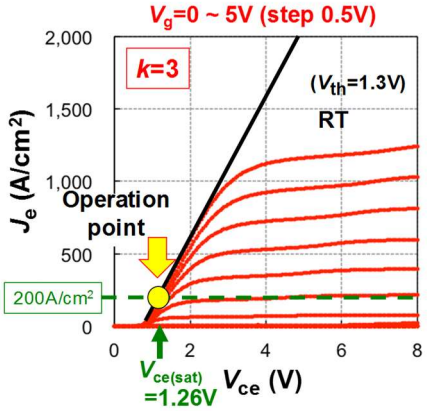

Figure 4 J_e-V_{ce} characteristics of an IGBT with k=3 based on the proposed scaling principal.

4. Conclusions

We have fabricated the 3D scaled IGBT with key size parameters 3 times smaller (k=3) than those of the current commercial products (k=1) by carefully designing the scaling scheme in which the tradeoff between performance and manufacturability is considered. It has been experimentally confirmed for the first time that significant $V_{ce(sat)}$ reduction is achieved by scaling the IGBT both in lateral and vertical dimensions with decreasing the gate voltage.

Acknowledgements

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