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Potential of the 0.35 μm CMOS gate driver technology for the GaN power devices

Shohei Miyano, Takafumi Akagi, Seiya Abe, Satoshi Matsumoto

Kyushu Institute of Technology
1-1 Sensui-cho Tobata-ku, Kitakyushu-shi, Fukuoka 804-8550, Japan
Phone: +81-93-884-3234 E-mail: q349531s@mail.kyutech.jp

Abstract

This paper presents potential of 0.35 μm CMOS gate driver for GaN power devices and the GaN power device based DC-DC converter through experimental and circuit simulation results. The simulation results show that optimized 0.35 μm CMOS gate driver and 3D stacked power SoC improves the efficiency to 94% at 30MHz and power handling capability of the DC-DC converter.

1. Introduction

Recently, POLs (point of load) has been attracting attentions because it can realize high efficiency and stable power supply. The one of the most important concerns related to POLs is to increase the switching frequency in order to reduce the volume POL and fast response. GaN power devices are attractive because it can operate high efficiency at high frequency switching [1, 2]. However, the conventional assembly technology cannot take advantage of GaN power devices at high frequency due to parasitic impedance [3]. The power-Supply on chip (power-SoC), which integrates Si-LSIs and power devices with passive devices in one chip is also attracting attention [4]. It can realize downsizing of the power supply and improve system efficiency. In the conventional power-SoCs are developed based on Si-LSI technology and it faces a problem of the efficiency at high frequency switching. We previously proposed 3D stacked power-SoC, which stacks GaN power devices, Si-LSI and passive components to improve the efficiency of the power SoC at high frequency[5]. The 3D stacked power SoC can minimize the parasitic inductance and improves the efficiency. In such a scheme, we demonstrated the Si based multi-tens MHz gate driver IC, which is one of key parts of high-frequency POL, for GaN power devices and DC-DC converter using developed gate driver IC [6].

In this paper, we explore 0.35 μm CMOS gate driver technology for GaN power devices using experimental results and circuit simulations. We also show the potential of the 3-D stacked power SoC using 0.35 μm CMOS gate driver IC technology.

2. Design consideration of gate driver IC

Figures1 and 2 compare the experimental and simulated waveforms for high side and low side gate driver. The simulated waveforms take into consideration of wiring impedance. The simulated waveforms close to experimental results. In the simulations, we taking into consideration of the wiring impedance used in Fig. 2 to enhance the accuracy of the simulations.

Table I shows the comparison of peak efficiency of the DC-DC converter obtained by experimentally and simulations. The maximum efficiency of the fabricated one is 59.2% when output current is 50mA[6]. The lower efficiency is caused by driver IC and assembly technology. The loss caused by ringing is largest, this will be improved by introducing 3-D stacked power SoC because ringing is caused by parasitic impedance. For the gate driver IC, loss cased by dead time is the largest[6]. The dead time of 7 ns is larger for 30 MHz switching and the longer dead time is caused by using external capacitor to generate dead time. Further more, there are some features to be improved.

A block diagram of the optimized gate driver IC presented in this paper is shown in Fig. 4. We assume to employ 0.35μm CMOS triple well process. We assumed to use EPC2040 as a switching device [7].

The maim features are

- Introducing on chip dead time generator and adjuster instead of external parts
- Increasing high-side and low-side gate drive current to realize appropriate rise time and fall time for 30MHz switching
- Negative bias for low side switch to prevent self turn-on

Table I Peak efficiency of DC-DC converter(Iout:50mA)

	Efficiency(%)
Experiment	59.2
Simulation	61.8

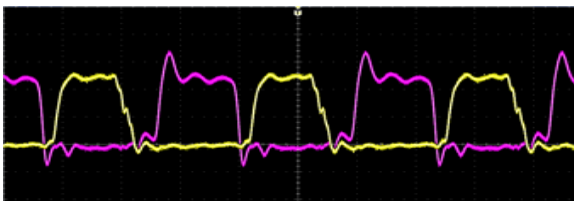

Fig.1 Experimental waveform of high side and low side

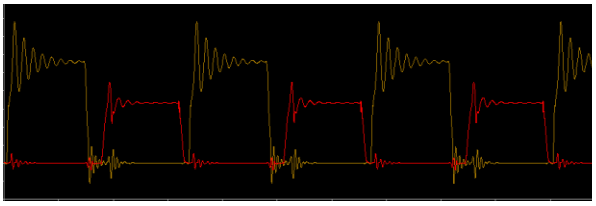

Fig.2 Simulated waveform of high side and low side

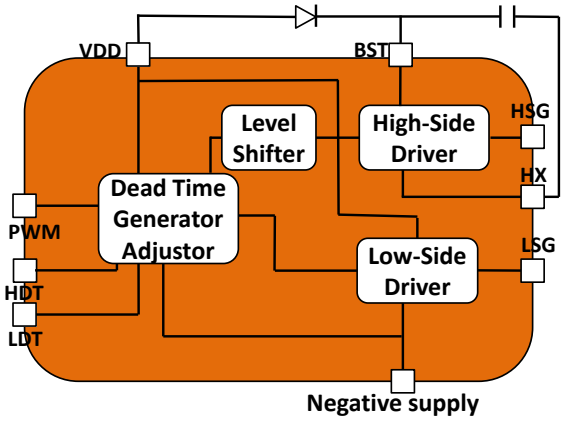

Fig.3 Block diagram of gate driver

In the optimized circuit, the dead time is generated by decreasing the duty ratio only for the low side. In addition, we optimize bootstrap capacitance. [8]

Table II compares the electric characteristic of DC-DC converter using optimized gate driver and previously developed one [5]. The electrical characteristics of the optimized gate driver IC are obtained by circuit simulation. From the results of optimization, high side rise time and fall time reduce to one third and those of low side also reduce to less than one fifth. In addition, we are successful to shorten the dead time by one tenth. These improvements are appropriate for 30MHz switching and improve the efficiency. In addition, these extend the operating range such as duty ratio.

Table II Electric characteristic of DC-DC converter

Description	Experiment [5]	optimized
Input voltage(V)	3.3	3.3
Output voltage (V)	1.65	1.65
Frequency (MHz)	30	30
Bootstrap capacitance (uF)	0.056	0.056
High side rise time	1.5ns	450ps
High side fall time	1ns	330ps
Low side rise time	1.2ns	220ps
Low side fall time	1.4ns	150ps
Dead time(high side)	7ns	550ps
Dead time(low side)	3ns	300ps

3. Electrical characteristics of buck converter

Dependence of efficiency of DC-DC converter which uses above mentioned optimized gate driver on output current at a switching frequency of 30MHz is shown in Fig. 5. In this case 3D power SoC is assumed. Our previously reported results are also shown in this figure [5]. Maximum

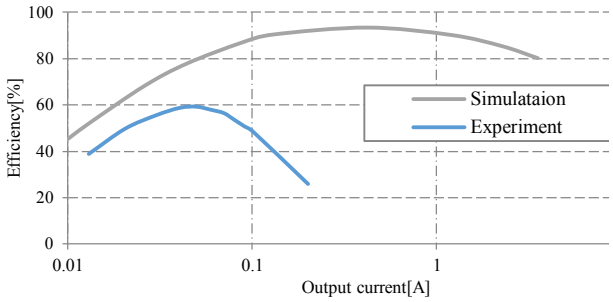

Fig. 4 Efficiency of DC-DC converter (Vin: 2.5V, Duty: 50%)

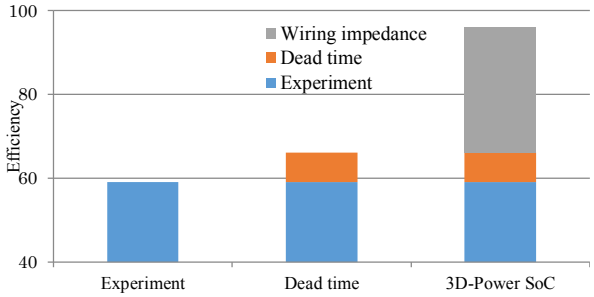

Fig.6 Contribution for efficiency improvement.

efficiency improves to be 94% when output current is 500mA and output current increases.

Figure 6 shows contribution for improvement of efficiency. Reducing the dead time increases the efficiency by 7%. Introducing the 3D stacked improves the efficiency by 30% because it can minimize the wiring impedance.

4. Conclusions

We clarify the potential of 0.35μm CMOS based gate driver IC for GaN power device and DC-DC converter using experimental results and circuit simulation. The efficiency of more than 90% is expected at switching frequency of 30 MHz when we introduce 3D stacked power SoC and improved gate driver IC. The improvement of performance of gate driver IC is indispensable to realize efficiency of more than 90% at 30 MHz swiching.

References

[1] D. Reusch and J. Strydom, Applied Power Electronics Conference 2016 (2016)745.
[2] A.Lidow, Power SoC 2016, Plenary Session 3 (2012)192.
[3] D.Reusch, Virginia Polytechnic Institute and State University Doctor thesis (2012) 192.
[4] http://pwrsocevents.com/pwrsoc-2014-presentations/
[5] K. Hiura, Y. Ikeda, Y. Hino, and S.Matsumoto, Japanese JJAP, vol.56, 04CR13, 2017.
[6] T.Akagi, S.Miyano, S.Abe, S.Matsumoto, Applied Power Electronics Conference 2018(2018) 2062
[7]http://epc-co.com/epc/Products/eGaNFETsandICs/EPC2040.aspx
[8]http://www.infineon.com/dgdl/Infineon-dt98-2j.pdf-ANv01_00-JA.pdf?fileId=5546d46256fb43b3015756f4cf4643fb