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Vertical-type 2DHG Diamond MOSFETs

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Abstract

A vertical type device, which has perpendicular conduction paths to device substrates, is advantageous for power devices. We fabricated vertical-type 2 dimensional hole gas (2DHG) diamond metal-oxide-semiconductor field-effect transistors (MOSFETs) with trench structures. Trench structure was fabricated by inductive coupled plasma reactive ion etching and trench side-wall can be used for p-channel. Characteristics of vertical-type 2DHG diamond MOSFETs were comparable to those of lateral-type 2DHG diamond MOSFETs.

1. Introduction

We fabricated vertical-type 2DHG diamond MOSFETs using 2DHG layer for channel. Al_2O_3 layer has been used for gate insulator [1,2] for diamond MOSFET and passivation layer [3] on the 2DHG layer on hydrogen terminated diamond surface. Using high temperature atomic layer deposition (ALD) Al_2O_3[4] , the 2DHG layer has been formed without unstable adsorbates and showed stable hole conduction up to 800K [4,5]. In lateral-type devices, we have reported high breakdown characteristics (~2000 V) [6,7] and stable operation in wide temperature (10K~673K) [6]

The 2DHG formed by ALD Al_2O_3 is independent on crystal orientation, so can be fabricated on the trench side-wall. A proto-type vertical FET devices with 2DHG channel and drift region have been reported.

In this paper, we fabricated vertical-type 2DHG diamond MOSFETs whose current density is 2 orders of magnitude higher than the previous work [8]. Current density and on/off ratio at room temperature (RT) are comparable to lateral-type 2DHG diamond MOSFETs.

2. Results

The cross-sectional view of the vertical-type 2DHG diamond MOSFETs is shown in Fig.1. Nitrogen-doped layer is fabricated between undoped layers deposited on p^+-type diamond substrate by microwave plasma chemical vapor deposition (MPCVD). Additional nitrogen doped layer plays a part in blocking leakage current which flows in the direction perpendicular to the substrate and was fabricated at 1 µm depth with ~10^{19} cm^{-3} . 4 µm depth trench structure was formed by inductive coupled plasma reactive ion etching (ICP-RIE) with 150-nm-thick MgO mask. A 200 nm regrowth undoped diamond layer was deposited by MPCVD to cancel surface damages by etching and to form stable 2DHG layer. The gate length was fixed to 4 µm, and the total length between gate and drain, which corresponds to the effective drift length L_{GD}, was ~5µm. We defined the region between gate edge and trench top edges and trench sidewall as the drift region.

Fig. 2 and 3 show I_{DS}-V_{DS} characteristics and I_{DS}-V_{GS} characteristics at V_{DS} of −10 V at RT, respectively. From fig.2, maximum current density at V_{DS} of −10 V and −50 V were −49 mA/mm and 200mA/mm, respectively. Maximum drain current density is about 1 orders of magnitude higher than the previous vertical FET [8] and is almost equal to lateral type 2DHG diamond MOSFETs [6] in a similar scale. The threshold voltage (V_{th}) determined from I_{DS}-V_{GS} characteristics was 18.2 V and this value is also close to that of lateral-type device. In off state (V_{GS}~25 V), I_{DS} was approximately 10^{-7} mA/mm for RT operation and the on/off ratio of this device was over 8 orders of magnitude, and this value is also comparable to lateral-type device. This result shows that ~50-nm-thick nitrogen doped layer well blocked the substrate leakage current. Fig.4 shows I_{DS}-V_{DS} characteristics of measured and simulated results. Measured I_{DS}-V_{DS} curve was reproduced by device simulation based on the two-dimensional negatively charge sheet model [6]. The optimal charge density at the Al_2O_3/C-H diamond interface and carrier mobility at lateral channel and vertical channel at trench structure were -6.7×10^{12} cm^{-2} and 95 cm^2/Vs, -6.0×10^{12} cm^{-2} and 47 cm^2/Vs, respectively. Fig.5 shows current density at V_{DS} and V_{GS} of −50 V and −20 V of five devices in the range of RT–300 ℃. Although the current density at 300 ℃ decreased comparing to RT, that was stable under 200 ℃. Fig. 6 shows I_{DS}-V_{GS} characteristics at V_{DS} of −10 V in the range of RT–300 ℃. At RT and 150 ℃, the on/off ratio is about 8 and 7 orders of magnitude, respectively, and current density reached the lower measurement limit (~10^{-7} mA/mm) in off state. At 200 ℃, leakage current increased comparing with RT, but on/off ratio was still high as ~5 orders of magnitude. At high temperature (~300 ℃), drain current dependence on gate voltage dropped down and on/off ratio was ~1 order of magnitude, indicating that this device could not work properly at high temperature (over 300 ℃) , because the blocking layer (N doped thin layer) is not thick enough. .

3. Conclusions

We fabricated vertical-type 2DHG diamond MOSFETs,

whose characteristics are comparable to lateral-type device by the nitrogen-doped layer. Vertical-type 2DHG diamond MOSFETs we modulated even in the high temperature up to 200 °C.

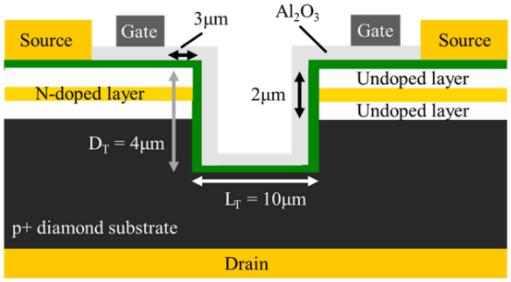

Fig. 1. The cross-sectional illustration of vertical-type C-H diamond MOSFETs.

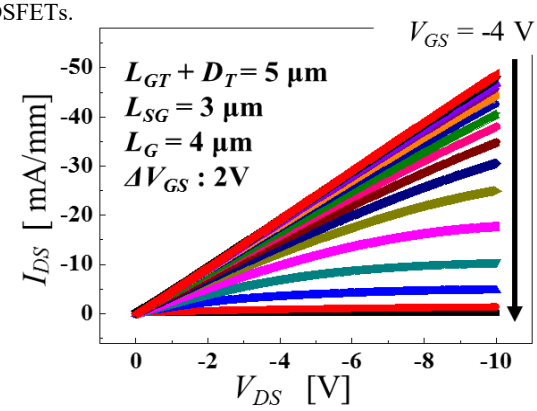

Fig. 2. I_{DS}-V_{DS} characteristics at room temperature. Current density was 49 mA/mm at V_{DS} and V_{GS} of –10 V and −4 V, respectively.

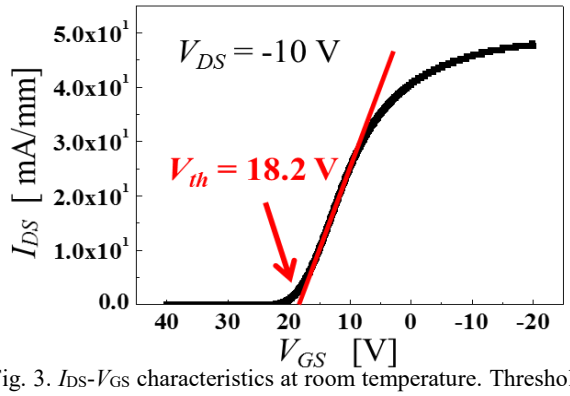

Fig. 3. I_{DS}-V_{GS} characteristics at room temperature. Threshold voltage V_{th} was 18.2 V.

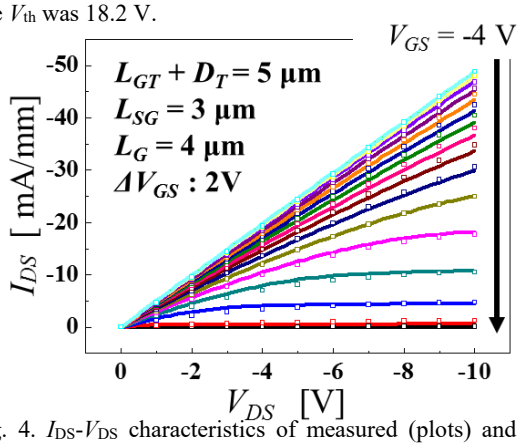

Fig. 4. I_{DS}-V_{DS} characteristics of measured (plots) and simulated (solid lines) results.

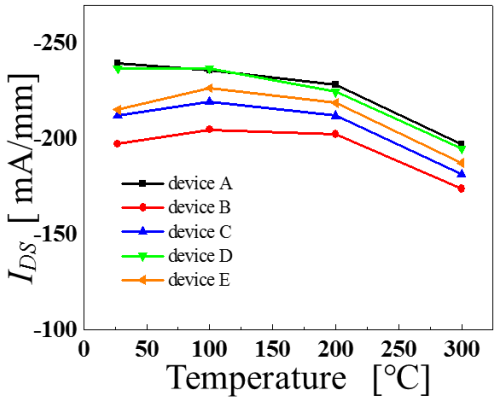

Fig. 5. Temperature dependence on maximum current density at V_{DS} and V_{GS} of −50 V and −20 V, respectively, at room temperature–300 °C

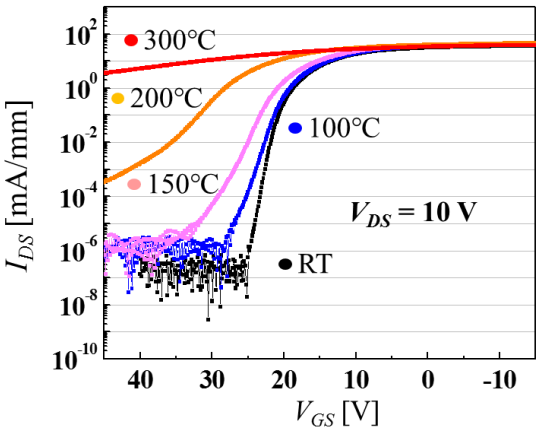

Fig. 6. Temperature dependence of I_{DS}-V_{GS} characteristics at V_{DS} of −10 V.

Acknowledgements

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