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High-performance E-mode recessed GaN Power MIS-HEMT with La-silicate gate insulator

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Abstract

An E-mode GaN MIS-HEMTs using multilayer La_2O_3/SiO_2 as gate insulator is investigated for high power application. The multilayer La_2O_3/SiO_2 composite oxide transformed to La-silicate amorphous phase after PDA at 600ºC for 5 minutes with good interface between oxide and AlGaN. The device exhibits a small subthreshold swing (SS) of 104 mV/decade, a low ON-resistance of 7.6 Ω·mm, high $I_{DS,max}$ of 752 mA/mm, and high $G_{m,max}$ of 210 mS/mm.

1. Introduction

GaN-based materials with high carry density and high bandgap are promising materials for high power device applications [1]. The GaN enhancement-mode (E-mode) metal-insulator-semiconductor high-electron-mobility transistor (MIS-HEMT) has been widely investigated for high power application due to the safety issue and simplicity in circuit design as compared to D-mode devices [2]. In order to improve performance of E-mode devices, gate insulator is a good way to achieve some goals, such as lower gate leakage current or more positive threshold voltage. Composite oxide structures have been studied as gate insulator for next-generation device applications in recent years, and La-silicate is known to have excellent interface property with Si substrate with low Dit [3].

In this study, we improved the performance of the recessed E-mode GaN Power MIS-HEMT by introducing new gate insulator [4]. Recessed GaN MIS-HEMTs were fabricated with La-silicate gate insulator, and their excellent performance was compared with published data of different gate insulators.

2. General Instructions

Experiment

The fabrication process of this device is shown below. First, Au(100nm)) /Ni(25nm)/Al(120nm)/Ti(20nm) was deposited by E-gun evaporator and thermally alloyed at 800 ^{0}C for 1 minutes to form S/D contacts. Then, the device isolation and gate recess were carried out by using inductive coupled plasma (ICP) etching with Cl_2 gas subsequently. The mesa isolation etching depth is 200 nm in this study. After that, multilayers La_2O_3(0.5nm)/SiO_2(0.5nm)×10 were deposited on the wafer by molecular beam deposition. Then, post deposition annealing (PDA) at 600°C was performed for 5 min to form a La-silicate film. Finally, an 100 nm SiNx layer was deposited as the passivation layer, and Au(200nm)/Ni(50nm) gate metal was deposited by E-gun evaporator with the gate length of 0.2μm defined by e-beam lithography. The structure of the La-silicate GaN MIS-HEMT and are shown in Fig. 1.

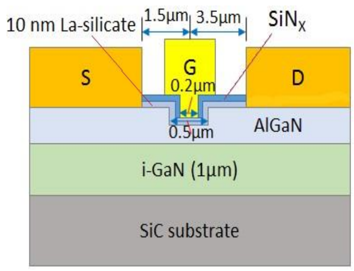

Fig. 1: the structure of the device

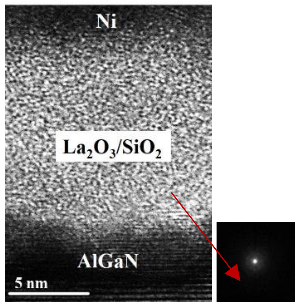

Fig. 2: TEM Image of the La-silicate on GaN device

Result and Discussion

Small hysteresis was achieved for La_2O_3/SiO_2 on AlGaN caused by forming La-silicate interfacial layer on AlGaN after PDA at 600^{0}C for 5 minutes. Cross-sectional TEM image and Nano-Beam Diffraction (Fig. 2) of the 10 nm La-silicate on GaN device indicates that the La-silicate film remained amorphous due to its higher crystallization temperature which results in device with lower leakage current and excellent interface.

The subthreshold swing (SS) of 104 mV/decade and $I_{ON}/I_{OFF} = 10^7$ at V_{DS} = 10 V (Fig. 3), the low gate leakage

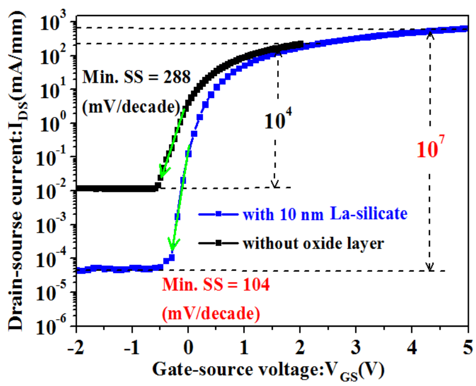

Fig. 3: Transfer characteristic of GaN E-mode HEMT and MISHEMT with La-silicate stack gate insulator.

current and the high breakdown voltage of 670 V was achieved for the E-mode La-silicate GaN MIS-HEMTs with 2.2 nm equivalent oxide thickness (EOT). Furthermore, the high $I_{DS,max}$ of 752 (mA/mm) at V_{GS} = 6V and low ON resistance of 7.6 mΩ·mm, and the high $G_{m,max}$ of 210 (mS/mm) were obtained (Fig. 4).

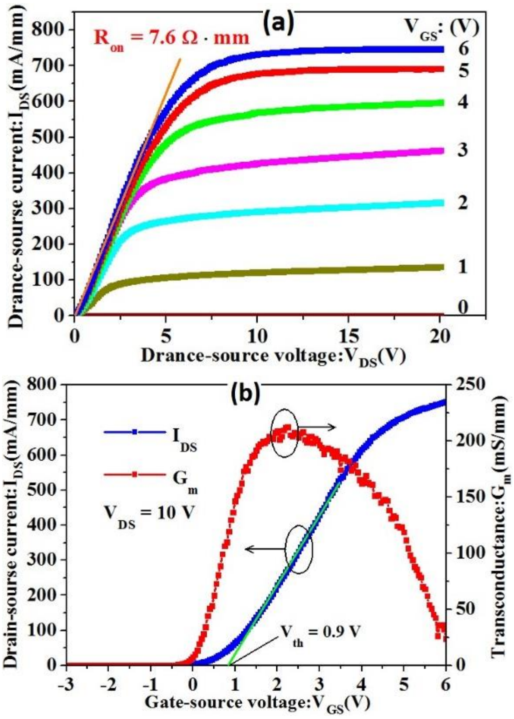

Fig. 4: (a) I_{DS}-V_{DS}, and (b) I_{DS}/G_m-V_{GS} characteristics of gate recessed MIS-HEMT with La-silicate gate insulator.

To further investigate the V_{th} hysteresis stability, the sweep transfers characteristics were measured by pulsed I_{DS}-V_{GS} as shown in Fig. 5, which shows there is only a slight V_{th} shift and nearly no V_{th} hysteresis when V_{DS} swept from 3V to 0.5V for the gate recessed GaN MIS-HEMT with La-silicate gate insulator. The V_{th} stability can be attributed to the decrease of the Ga-O bond after annealing and the low fixed charge density in the amorphous La_2O_3/SiO_2 dielectric film. The low interface trap density and the excellent oxide quality can be attributed to the formation of the La-silicate gate insulator.

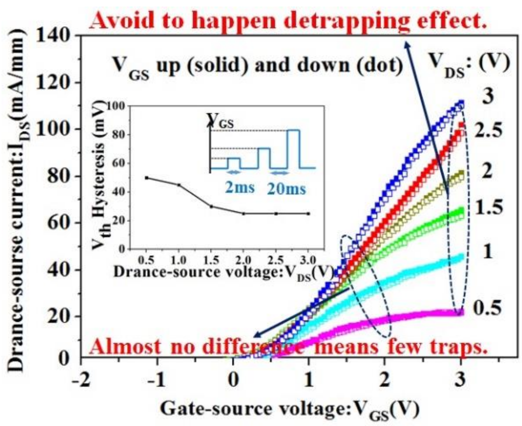

Fig. 5: Transfer sweep measured with different V_{DS} from 0.5 V to 3 V by pulse mode of normally-off MIS-HEMT

Compared with other devices (Table I), the E-mode La-silicate GaN MIS-HEMT shows high with current density, high with breakdown voltage, lower ON resistance, and small hysteresis demonstrating the potential for high power application as shown in Table I

Table. I: Comparison of DC characteristics of the La-silicate with others gate dielectric GaN MIS-HEMTs.

	This work	Ref. [5]	Ref. [6]	Ref. [7]
Oxide/ Thickness (nm)	La-silicate/ 10	Al_2O_3/ SiO_3 7/9	Al_2O_3/AlN 22/1	Al_2O_3/ 16
L_G (μm)	0.2	0.12	1	1
V_{TH} (V)	0.9	0.8	1.2	1.5
I_{DS}, max (mA/mm)/ L_{GD} (um)	752/3.4	530/10	660/2.5	693/5
Gm, max (mS/mm)/ L_{GD} (um)	210/3.4	~100/10	79/2.5	166/5
Hysteresis (mV)	50	-	700	~700
Ron (Ω•mm)	7.6	13.8	11	5.2
Min. SS (mV/dec.)	104	86	-	-
Ion/Ioff	10^7	10^8	10^{10}	10^8
BV(V)/ L_{GD}(μm)	440/3.4 @1mA/mm 670/10 @1mA/mm	565/10 @0.6uA/mm	465/15 @10uA/mm	408/5 @1mA/mm 860/10 @1mA/mm

3. Conclusions

E-mode GaN MIS-HEMT with annealed La-silicate stack insulator is investigated. The device shows a threshold voltage of 0.9V, a $I_{DS,max}$ of 752 mA/mm, a $G_{m,max}$ of 210 mS/mm and an off-state breakdown of 670 V. Moreover, the device demonstrated a low threshold voltage hysteresis and exhibited less than 50mV threshold voltage (V_{th}) shift with gate bias voltage sweep from 0.5 to 3 V for the E-mode devices. The composite insulator La_2O_3/SiO_2 is a very promising gate stack insulator for the E-mode AlGaN/GaN MIS-HEMTs for high power application.

Acknowledgements

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