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Enhancing the Performance of Ni-$In_{0.53}Ga_{0.47}As$ MOSFETs Using Post Silicon Dopant Process

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Abstract

In this paper, we demonstrate an improvement on the Ni-$In_{0.53}Ga_{0.47}As$ MOSFETs' performance with post silicon dopant (PSD) process. The electron Schottky barrier height (SBH) of Ni-InGaAs device can be adjusted by introducing Si implanted dopants into metal alloy source/drain (S/D) regions. This technique improved the on-state current (I_{DS} = 102.9 μA/μm at V_{GS} = 2 V) and transconductance (G_m = 65.3 μS/μm at V_D = 1 V) of MOSFET devices, as compared to conventional n^+/p junction and normal Ni-InGaAs MOSFET devices. In addition, the S/D series resistance (R_{SD}) has been suppressed by more than 50% whilst remaining a low sheet resistance (R_{sheet}) of 21.6 Ω/□.

1. Introduction

III–V compound semiconductors have been considered as new channel materials for the future extremely scaled complementary metal oxide semiconductor (CMOS) due to the expected high injection velocity and electron mobility [1]-[3]. However, one of the key technical challenges in realizing high performance III–V nMOSFETs is the reduction of source/drain (S/D) resistance R_{SD} [4]. Due to their low dopant solid solubility and high diffusivity, a high R_{SD} is disappointing the performance of III-V based MOS devices. Recently, the utilization of metal alloy S/D structure in InGaAs MOSFET has been presented as a promising approach to overcome this limitation. The R_{SD} can be further suppressed by modulating In content in the Ni-$In_xGa_{1-x}As$ MOSFETs [5]. However, the very small bandgap of high In content $In_xGa_{1-x}As$ materials may be a drawback owning to the potentially high band to band leakage current. In this article, we propose a post silicon (Si) dopant (PSD) process to realize a small electron Schottky barrier height (SBH) in Ni-$In_{0.53}Ga_{0.47}As$ structure, and examine the electrical properties of the $In_{0.53}Ga_{0.47}As$ MOSFETs devices prepared utilizing this technique.

2. Experimental Procedure

The epitaxial structure used in this study consisted of 50 nm p-$In_{0.53}Ga_{0.47}As$ (5 x 10^{16} Be doped) channel layer and 100 nm p^+-InP buffer layer on the p^{++}-InP substrate grown by solid source molecular beam method. The gate-first self-aligned process was used to fabricate the Ni-$In_{0.53}Ga_{0.47}As$ MOSFETs with PSD technique as described in Fig. 1. After degreasing in acetone and isopropanol, the chemical pretreatments were carried out in 4% HCl solution and 10% $(NH_4)_2S$ solution, respectively. Then, a 10-nm Al_2O_3 film was deposited as the gate oxide by Atomic Layer Deposition (ALD) at 250 ˚C. After that, post deposition annealing (PDA) was performed at 400 ˚C for 2 minutes in forming gas. A 100-nm TiN metal gate electrode was deposited by physical vapor deposition. Gate pattern was defined via optical lithography and TiN dry-etching was conducted using inductively coupled plasma reactive ion etching. After that, a 30-nm Ni layer for S/D was evaporated by e-beam evaporation, followed by rapid thermal annealing (RTA) at 250 ˚C for 1 min to form the Ni-InGaAs alloy in the S/D regions. Unreacted Ni was removed by selective wet etching with HCl. Next, the post implanted Si dopants were examined with different implantation energies and rapid thermal annealing (RTA) temperatures to realize small SHB. Finally, Au/Ge/Ni/Au S/D Ohmic and AuBe backside contact were formed by e-beam evaporation, and post metallization annealing was finally performed at 300 ˚C in 30 seconds in N_2.

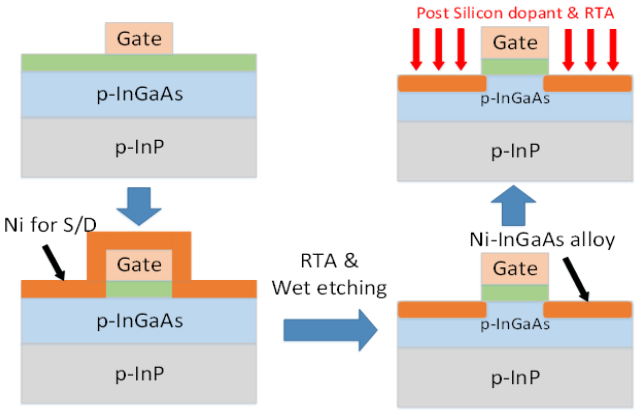

Fig. 1 Schematic diagram of device structure and process flow for the Ni-$In_{0.53}Ga_{0.47}As$ MOSFET fabrication with PSD technique.

3. Results and Discussion

Fig. 2(a) and (b) show the current-voltage (*I-V*) characteristics of the Ni-$In_{0.53}Ga_{0.47}As$/p-$In_{0.53}Ga_{0.47}As$ diodes and the schematic diagram of the junction structure, respectively. For various PSD conditions (implantation energy of 10 and 20 keV; RTA temperature of 400 and 450 ˚C for 30 sec), it is found that higher RTA temperature and lower implantation energy can help to decrease the SBH. The lowest value of SHB extracted from the *I-V* characteristics [6] was approximately 0.404 eV, which was beneficial in lowering the resistance and increasing I_{DS}. Electron SBH and ideality factor at various PSD conditions are shown in Fig. 3. It is revealed that samples with lower SHBs exhibited higher ideal factors. Fig. 4 confirms the influences of SBH engineering process on the electrical characteristics of Ni-InGaAs MOSFETs. Higher I_{DS} current can be realized with lower electron SBH structure.

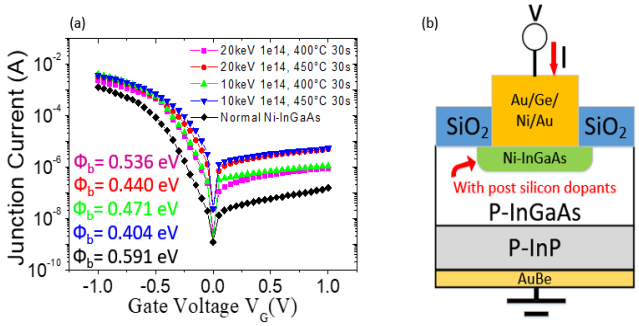

Fig. 2 (a) *I-V* electrical characteristics of Ni-$In_{0.53}Ga_{0.47}As$/p-$In_{0.53}Ga_{0.47}As$ diodes fabricated with PDS process. (b) The schematic diagram of the junction cross section.

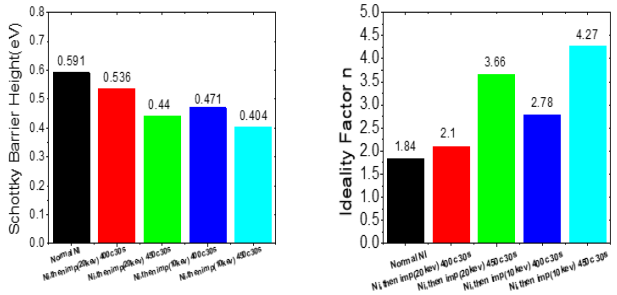

Fig. 3 (a) Electron Schottky barrier height and (b) ideality factor for diodes structures fabricated with a variety of PDS condition.

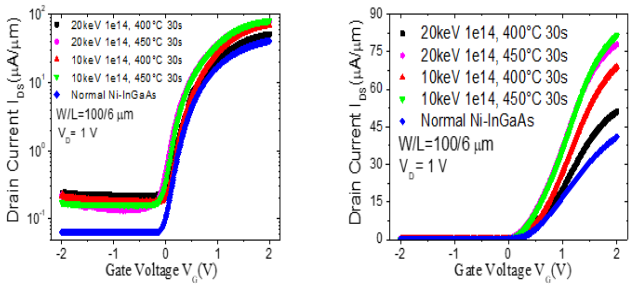

Fig. 4 Transfer characteristics of Ni-InGaAs MOSFETs fabricated with PSD technique in (a) logarithm and (b) linear scale.

In Fig. 5(a) and (b), Ni-InGaAs MOSFET with PSD process showed lower sheet resistance R_{sheet} (21.6 Ω/□) and R_{SD} (1.216 kΩ-μm). From Fig. 5(c) and (d), the electrical performance of the $In_{0.53}Ga_{0.47}As$ MOSFET with L_G of 6 μm and W_G of 100 μm fabricated by PSD process was compared to those fabricated by other techniques. The device with PSD process provided 142% drive current and 108% transconductance enhancements as compared to other results. This device showed I_{DS} of 102.9 μA/μm at V_{GS} = 2 V and V_{DS} = 2 V, and $G_{m,max}$ of 45.42 μS/μm at V_{DS} = 1 V.

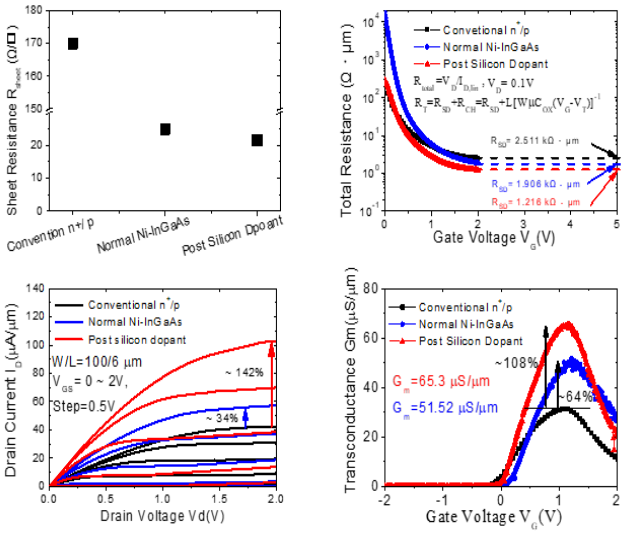

Fig. 5 (a) The sheet resistance and (b) the total resistance in the linear regime (V_D = 0.1 V) as a function of gate voltage for InGaAs MOSFET with or without PSD process. (c) Output and (d) transfer characteristics of InGaAs MOSFETs fabricated with and without PSD process.

3. Conclusions

We improved the performance of $In_{0.53}Ga_{0.47}As$ MOSFET with PSD technique through the electron SBH adjustment. The results show that the InGaAs MOSFETs with PSD process outperformed the conventional n^+/p S/D and normal Ni-alloy S/D devices. The low R_{sheet}, R_{SD} and the high output performance observed with PSD devices are attributed to the small electron SBH. This work proposed a potential SBH engineering process in order to push up the performance of III-V based MOSFET devices.

Acknowledgements

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References

[1] S. Takagi *et al.*, IEEE Trans. Elec Dev. **55** (2008) 21.
[2] J. J. Gu *et al.*, Appl. Phys. Lett. **99** (2011) 112113.
[3] J. J. Gu *et al.*, *IEEE International Electron Devices Meeting* (2011) 33.
[4] H. Tsuchiya *et al.*, IEEE Elec. Dev. Lett. **31** (2010) 365.
[5] S. Takagi *et al.*, Solid State Electron. **51** (2007) 526.
[6] D. K. Schroder, *Semiconductor Material and Device Characterization*. Hoboken, NJ, USA: Wiley, 2006.