Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp687-688

O-1-01 (Invited)

Accurate Evaluation of Fast Threshold Voltage Shift for SiC MOS Devices Under Various Gate Bias Stress Conditions

Mitsuru Sometani[1], Mitsuo Okamoto[1], Tetsuo Hatakeyama[1], Yohei Iwahashi[1], Mariko Hayashi[1,2], Dai Okamoto[3], Hiroshi Yano[3], Shinsuke Harada[1], Yoshiyuki Yonezawa[1], and Hajime Okumura[1]

[1] National Institute of Advanced Industrial Science and Technology, 16-1 Onogawa, Tsukuba, Ibaraki 305-8568, Japan
Phone: +81-29-861-8742 E-mail: m.sometani@aist.go.jp
[2] DENSO CORPORATION, 500-1, Minamiyama, Komenoki-cho, Nisshin, Aichi 470-0111, Japan
[3] University of Tsukuba, 1-1-1 Tennodai, Tsukuba, Ibaraki 305-8573, Japan

Abstract

Fast measurement methods were introduced to accurately evaluate the threshold voltage (V_{th}) shift under various gate bias stress conditions for SiC metal–oxide–semiconductor (MOS) devices. By suppressing the stress relaxation during measurements, large V_{th} shifts were observed compared with conventional methods. The effects of those fast V_{th} shifts on the drain current and V_{th} under the AC gate bias stress were examined.

1. Introduction

Silicon carbide (SiC) has attracted much interest for use in high-voltage and high-temperature power devices owing to its wide bandgap, high thermal conductivity, and high breakdown electric field [1]. However, low channel mobility and the threshold voltage (V_{th}) shift under positive and negative gate bias stresses due to the large number of interface and near-interface defects are major issues for SiC metal–oxide–semiconductor (MOS) field-effect transistors (FETs) [2]. A positive V_{th} shift reduces the drain current (I_d) during the on-state, and a negative V_{th} shift stress causes unintentional turning on. Recently, we observed significantly large V_{th} shifts under various gate bias stress conditions with fast measurement methods [3, 4]. Fast V_{th} shifts should be a serious concern because their stress-time range and the on-state time of actual AC operation are very close. In this paper, we introduce methods to evaluate the fast V_{th} shift under positive and negative DC gate bias stresses. The effects of these V_{th} shifts on I_d and V_{th} during one pulse of an AC gate bias stress were investigated.

2. V_{th} shift under a positive DC gate bias stress

The V_{th} shift under a positive DC gate bias stress is generally measured by the sweep method [5, 6], where a drain current–gate voltage (I_d–V_g) curve is measured to determine V_{th} and a constant V_g is applied as the gate bias stress iteratively. I_d–V_g is measured from V_g = 0 V to above V_{th}, which typically takes approximately 10 s. Measuring I_d–V_g may cause the V_{th} shift to be underestimated owing to stress relaxation by charge de-trapping. To estimate the V_{th} shift without relaxation, we proposed a non-relaxation (NonRlx) method [7], where a constant V_g is continuously applied as a gate bias stress and a drain-source voltage (V_{ds}) is automatically adjusted to maintain a constant I_d by using standard source measure units (SMUs). Then, the measured V_{ds} is converted to the V_{th} as follows:

$$I_d = \frac{W}{L}\mu C_{ox}\left(V_g - V_{th}\right)V_{ds} \qquad (1)$$

where W is the gate width, L is the gate length, μ is the channel mobility, and C_{ox} is the oxide capacitance. The product of W/L, μ, and C_{ox} can be estimated from the slope of the I_d–V_g characteristics at the gate-stress voltage.

Figure 1 compares the V_{th} shifts measured by the sweep and NonRlx methods under a positive DC gate bias stress of +15 V. The oxide films of the MOSFETs were formed by thermal oxidation in dry O_2 followed by post-oxidation annealing (POA) in N_2O ambient. The V_{th} shift values measured by the NonRlx method were larger than those measured by the sweep method, especially in the extremely short stress-time region. For detailed investigation of the V_{th} shift in the short stress-time region, we used the high-speed non-relaxation (HS NonRlx) method with high-speed SMUs [3].

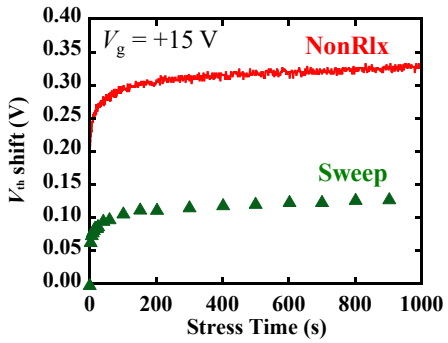

Fig. 1 Comparison of the V_{th} shifts measured with the sweep and NonRlx methods under a positive DC gate bias stress [7].

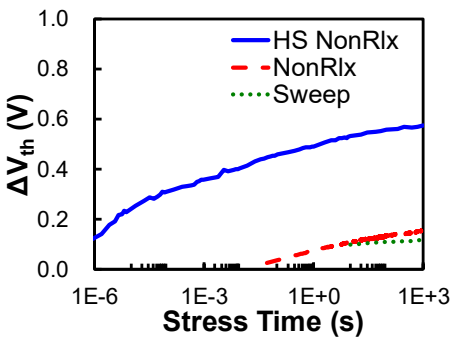

Fig. 2 V_{th} shift measured with the sweep, NonRlx, and HS NonRlx methods under a positive DC gate bias stress [3].

Figure 2 shows the V_{th} shifts measured by the sweep, NonRlx, and HS NonRlx methods. The oxide films of MOSFET were formed by thermal oxidation in dry O_2 followed by POA in NO ambient. An extremely large V_{th} shift was observed with the HS NonRlx method compared with the other methods. This result indicates that a large amount of charge trapping occurred in a short stress time.

3. V_{th} shift under a negative DC gate bias stress

V_{th} under a negative DC gate bias stress is also generally measured with a sweep method [8, 9]. However, owing to the positive V_g bias in the I_d–V_g measurement, the trapped holes induced by the negative gate bias stress recombined with the channel electrons, which results in a significant recovery of the V_{th} shift. To avoid this recombination of trapped holes with channel electrons, the shift of the flat band voltage (V_{FB}) was estimated from capacitance–voltage (C–V) measurements in the negative gate bias region. The V_{th} shift was then determined [10]. With this C–V method, a large V_g shift was observed compared with the sweep method. However, V_{FB} measurement typically takes about 10 s with a conventional LCR meter. This is close to the measurement time of the sweep method. Thus, the V_{th} shift should be underestimated, similar to measuring the V_{th} shift under a positive gate bias stress with the sweep method. Therefore, we used the fast C–V method with a constant-capacitance deep-level transient spectroscopy (CC-DLTS) measurement system to measure the V_{FB} within 10 ms [4]. Figure 3 compares the measured V_g shifts under a negative DC gate bias stress of −15 V with the sweep, C–V, and fast C–V methods. The V_g shift was defined as equal to the V_{th} and V_{FB} shifts. The oxide films of MOS capacitors and MOSFETs were formed by thermal oxidation in dry O_2 followed by POA in NO ambient. An extremely large V_g shift was observed with the fast C–V method compared to the other methods. This means that fast measurement is indispensable for both positive and negative gate bias stresses to clarify the mechanisms of trapping during stress and de-trapping during V_{th} measurement.

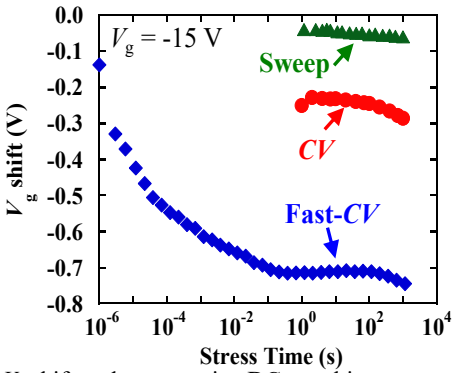

Fig. 3 V_g shift under a negative DC gate bias stress measured with the sweep, C–V, and fast C–V methods [4].

4. V_{th} shift under an AC gate bias stress

Under an AC gate bias stress, charge trapping and de-trapping occur simultaneously. Thus, the long-term V_{th} shifts show complicated behavior dependent on the frequency and duty cycle [11]. In addition, the V_{th} should also shift within one pulse short-term stress. Figure 4 shows the I_d and V_{th} shifts under an AC gate bias stress [3]. I_d appeared immediately after the on-state gate voltage was applied. Then, I_d decreased rapidly over time during the on-state within one pulse. The V_{th} shift converted from the I_d shift is extremely large. This phenomenon was also observed in commercially available SiC MOS devices [12]. The effects of long-term and short-term V_{th} shifts on the reliability during actual operation are not clear. Thus, careful investigation is necessary to bring out the full potential of SiC MOS devices.

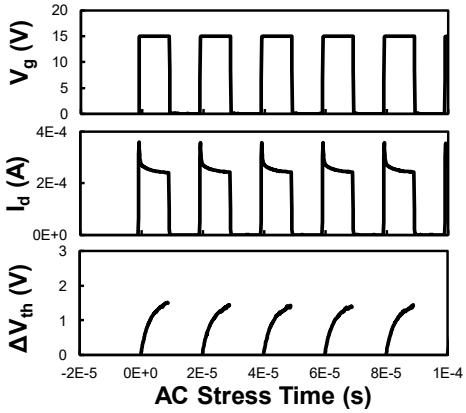

Fig. 4 V_{th} shift under an AC gate bias stress measured with the HS NonRlx method [3].

5. Conclusions

The HS NonRlx method and fast C–V methods showed large V_{th} shifts in a short stress time under positive and negative DC gate bias stresses compared with conventional methods. The results indicate that suppressing stress relaxation is indispensable to avoid underestimation of the V_{th} shift. The effects of these fast V_{th} shifts on the I_d shift during the on-state of AC operation were also investigated. A large decrease in I_d over time during the on-state within one pulse was observed.

Acknowledgments

This work was supported by Council for Science, Technology and Innovation (CSTI), Cross-ministerial Strategic Innovation Promotion Program (SIP), "Next-generation power electronics" (funding agency: NEDO). We gratefully acknowledge A. Otsuki and M. Takei of Fuji Electric Co., Ltd. for the helpful discussions.

References

[1] T. Kimoto, Jpn. J. Appl. Phys. **54**, 040103 (2014).
[2] Y. Fujino *et al.*, J Appl. Phys.**120**, 085710 (2016).
[3] M. Okamoto *et al.*, Mater. Sci. Forum **897**, 549 (2017).
[4] M. Hayashi *et al.*, submitted to SSDM2017.
[5] A. J. Lelis *et al.*, IEEE Trans. Electron. Devices **55**, 1835 (2008).
[6] J. Senzaki *et al.*, Mater. Sci. Forum **778-780**, 521 (2014).
[7] M. Sometani *et al.*, Jpn. J. Appl. Phys. **55**, 04ER11 (2016).
[8] J. Rozen *et al.*, J. Appl. Phys. **105**, 124506 (2009).
[9] M. Matsumura *et al.*, Jpn. J. Appl. Phys. **54**, 04DP12 (2015).
[10] Y. Katsu *et al.*, Mater. Sci. Forum **858**. 599 (2016).
[11] E. Murakami *et al.*, Jpn. J. Appl. Phys. **56**, 04CR11 (2017).
[12] M. Sometani *et al.*, Proc. of ISPSD'17, 395 (2017).