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Hole Trapping in SiC-MOS Devices Evaluated by Fast-*CV* Method

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Abstract

We demonstrated a fast-*CV* method for accurate evaluation of the number and location of holes trapped in a 4H-SiC metal-oxide-semiconductor (MOS) device under negative gate bias stress. Recombination and detrapping of the trapped holes are successfully suppressed using this method. It was found that a large number of holes trapped in a short-stress time are reduced by nitridation, and that the hole trapping in a long-stress time region is accelerated by an increase in temperature for the test. Based on the results, we determined the respective model for hole trapping and detrapping.

1. Introduction

Suppression of threshold voltage (V_{th}) shift under gate bias stress is an important factor for the reliability of SiC metal-oxide-semiconductor (MOS) devices. The positive V_{th} shift causes a reduction in the drain current during the on-state, and the negative V_{th} shift causes unintentional turn-on. The V_{th} shift occurs due to gate stress because channel charges are injected into gate oxide and/or interface states are generated. The injected charges near the SiO_2/SiC interface are transiently released after the gate bias stress is removed. Thus, the measured V_{th} shift reflects the number of remaining trapped charges during the gate-voltage sweep [1]. Actually, a large V_{th} shift was observed by high-speed V_{th} measurement for the positive bias stress test [1,2]. Therefore, the accurate number of trapped charge and their detrapping phenomena should be investigated prior to the V_{th} shift measurement.

There were few report on hole trapping by negative gate bias stress so far [3-5]. In this study, we establish a method to accurately estimate the number of holes trapped by negative gate bias, and clarify the mechanisms of trapping during stress and detrapping during V_{th} measurement. The influence of the nitridation process on the negative V_{th} shift is also discussed.

2. Experimental

N-channel MOS field-effect transistors (MOSFETs) were fabricated on a p-type epitaxial layer on a (0001) Si-face n-type 4H-SiC wafer. P-type MOS capacitors were also fabricated on a p-type epitaxial layer on a p-type 4H-SiC wafer. Gate oxide films with thicknesses of 50 nm were formed by thermal oxidation in dry O_2. Then, post-oxidation annealing (POA) in NO ambient was performed for 10, 60, and 120 min.

The V_{th} shift due to negative gate stress was measured by two methods: sweep method and fast-*IV* method. The number of trapped holes was measured by the *CV* method and fast-*CV* method, which we propose in this study. In the sweep method, the drain current vs. gate–source voltage (I_d–V_g) measurements to determine V_{th} and the constant V_g stress were iteratively performed on the MOSFETs using standard source measure units (SMUs). The V_{th} measurement performed using the sweep method typically requires approximately 10 s. However, in the fast-*IV* method, using high-speed SMUs, the V_{th} measurement requires approximately 10 μs. In the *CV* method, the constant V_g stress and capacitance–voltage (*CV*) measurements were iteratively performed on MOS capacitors using a conventional LCR meter in the depletion mode to estimate the flat band voltage (V_{FB}) [5]. The V_{FB} measurement typically takes approximately 10 s. However, in the fast-*CV* method proposed in this work, stress in a short time and high-speed measurement of V_{FB} within 10 ms were enabled using a constant-capacitance deep-level transient spectroscopy (CC-DLTS) measurement system.

A negative V_g stress of −15 V was applied for all evaluation methods in this work. When the holes are trapped in the bulk SiO_2 and/or the near-interface region, the V_{th} and the V_{FB} should be shifted by the same value. Thus, both the V_{th} and the V_{FB} shifts were defined as ΔV_g.

3. Results and Discussions

Figure 1 compares the ΔV_g values of the sample nitrided for 60 min, evaluated using four methods. The values of ΔV_g obtained using the methods based on the *CV* measurement are larger than those obtained by the methods based on the I_d–V_g measurement. Owing to the positive V_g bias for the I_d–V_g measurement, the trapped holes are recombined with channel electrons, resulting in the recovery of ΔV_g. However, in the methods based on the *CV* measurement, because V_{FB} shifts as ΔV_g are measured in the depletion mode, the recombination of trapped holes does not occur, resulting in large negative ΔV_g values. Moreover, extremely large ΔV_g values measured by the fast-*CV* method indicate that a large number of holes, which are trapped in a short time, rapidly detrap in a period between the stress and V_{FB} measurement. Thus, the fast-*CV* method is more effective in evaluating ΔV_g based on stress in a short time.

Figure 2 shows the POA time dependence of ΔV_g under negative V_g stress measured by the fast-*CV* method. The ΔV_g value of the sample with POA for 10 min significantly in-

creases within a short stress time of 10^{-4} s, but is saturated after that. This significant increase in ΔV_g in a short-stress time is suppressed in samples with POA times over 60 min. This result indicates that a large number of near-interface traps are generated by dry oxidation but almost disappear during nitridation. However, excess POA time causes a slight increase in ΔV_g in a long-stress time region over 10 s. As shown in Fig. 3, the ΔV_g value in such a region drastically increases with the temperature for the test, indicating that hole trapping in a long-stress time region is accelerated by temperature increase, while that in a short-stress time region is almost independent of the temperature.

We estimated the location of the observed hole trapping sites as shown in Fig. 4. Trapping sites with short time constants for trapping and detrapping, which are reduced by nitridation, might be located in the shallow energy level from the valence band edge of 4H-SiC near the interface region. Therefore, hole trapping and detrapping have almost no temperature dependence. However, hole trapping with long time constants, which appear with increasing temperature, might be located away from the interface and high energy level, in which the trapping requires a thermal excitation process. Another possibility is that the hole trapping sites were generated by electrical and thermal stress.

3. Conclusions

Hole trapping by negative gate bias stress was investigated using various measurement methods. The fast-*CV* method was effective in evaluating ΔV_g caused by stress in a short time. It was found that nitridation suppresses hole trapping induced by stress in a short time. Hole trapping in a long-stress time region was accelerated by temperature increase. We expect that the trapped holes, which number increased with temperature, are located away from the interface and high energy level.

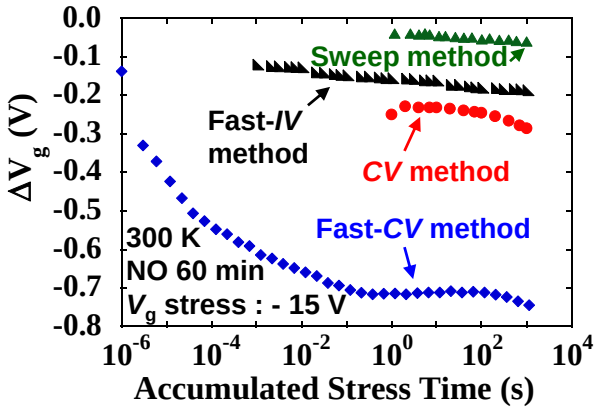

Fig. 1 Comparison of ΔV_g value under negative gate bias stress measured by various methods at 300 K.

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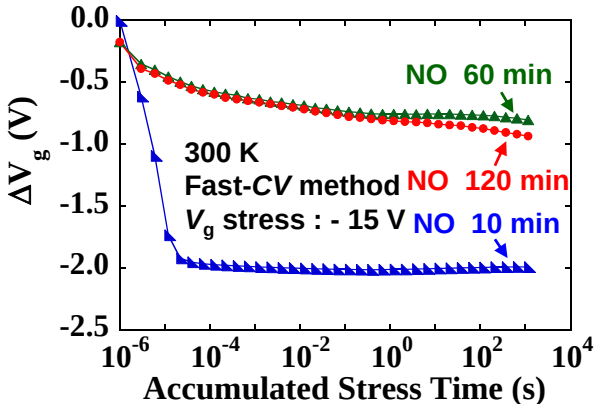

Fig. 2 Nitridation time dependence on ΔV_g under negative gate bias stress evaluated by fast-*CV* method.

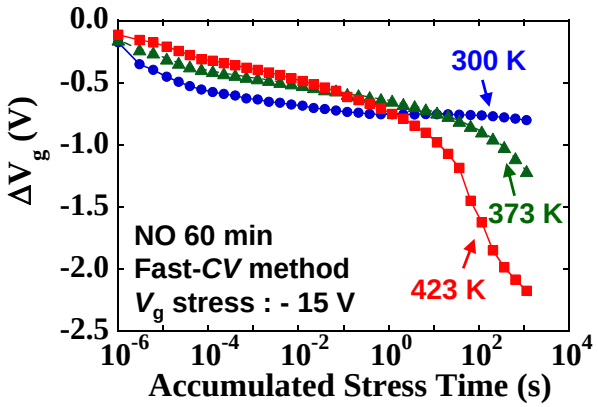

Fig. 3 Temperature dependence on ΔV_g under negative gate bias stress evaluated by fast-*CV* method.

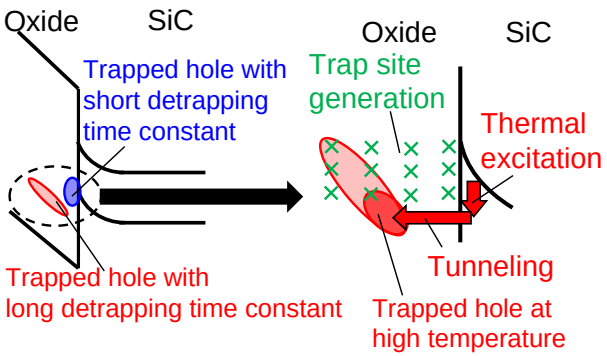

Fig. 4 Estimated location of hole trapping sites evaluated by fast-*CV* method.

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