Effect of Surface Roughness of Trench Sidewalls on Channel Mobility in 4H-SiC Trench MOSFETs

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Abstract

The effect of the surface roughness of trench sidewalls on electrical properties have been investigated for improving channel mobility in 4H-SiC trench MOSFETs. The surface roughness was evaluated by atomic force microscopy (AFM). The characteristics of channel mobility were analyzed based on the mobility model including optical phonon scattering. The results revealed that surface roughness scattering had small contribution to channel mobility, and there was no correlation between the experimental RMS values and surface roughness scattering. On the other hand, it was necessary to pay attention to the surface morphology from the view point of device reliability.

1. Introduction

One of the greatest challenges in 4H-SiC MOSFETs technology is reduction of the channel resistance by increasing channel mobility. Even though high values of mobility were achieved, the reported channel mobility is much lower than that anticipated from SiC bulk mobility (800-1000 cm² V⁻¹ s⁻¹), which suggests a need for deeper understanding what controls the carrier scattering limiting the inversion channel mobility in 4H-SiC MOSFETs.

We have investigated the channel mobility model in SiC trench MOSFETs which were expected to have lower on-state resistance than planar-type MOSFETs [1-3]. The temperature dependence of the effective mobility demonstrated that optical phonon scattering (μ_{OP}) was the essential factor in the mobility model and limited the total mobility at high temperature, in addition to Coulomb scattering (μ_C) and surface roughness scattering (μ_{SR}). Since the experimental results could be expressed by μ_{OP} , μ_C , and μ_{SR} , acoustic phonon scattering (μ_{AC}) was not included in our mobility model. Recently, to improve the device performance, the transformation of SiC trenches has been reported at very high temperatures, e.g., 1400 °C or more, in SiH₄/Ar [4] and in H₂ [5] ambient. However, the impact of surface morphology in trench MOSFETs on electron mobility is poorly understood.

In this study, we discuss the effect of the surface roughness in channel region of SiC trench MOSFETs on the electrical properties, especially on the channel mobility.

2. Experimental

The starting material was n-type 4H-SiC epitaxial layer grown on heavily doped n⁺-SiC (0001) substrate. The isolated one-cell trenched MOSFET with n-channel was fabricated in order to extract the channel resistance component and determine the effective channel mobility (μ_{eff}). The surface roughness of trench sidewalls was controlled by high-temperature annealing following the SiC etching. Nitridation was performed following deposition of a 75-nm-thick gate oxide in order to reduce the interface state. The drain current-gate voltage (I_D - V_G) and gate current-gate bias (I_G - V_G) characteristics were measured at the temperature in the range from -40 to 250°C. To quantify the surface roughness, AFM was employed.

3. Results and Discussion

Figure 1 shows the schematic image of the trench structures and AFM images in the channel region. The corresponding line profiles in parallel with the current direction and the RMS values were also shown. Based on the proposed mobility model, the mobility factors where the effective field (E_{eff}) was 1MV/cm measured at each temperature were shown in Fig. 2. The dependence of channel mobility on the gate bias with different RMS values was also shown in Fig. 3. The limiting factor of the mobility was $\mu_{\rm C}$ at a low measurement temperature ($\leq 25^{\circ}$ C), and μ_{OP} at a high temperature ($\geq 150^{\circ}$ C). In addition, surface roughness scattering had small contribution to the total mobility [6] and no correlation with experimental RMS values in the examined region. If $\mu_{\rm C}$ and $\mu_{\rm OP}$ are sufficiently improved, $\mu_{\rm SR}$ will have an impact. On the other hand, the large surface roughness which is perpendicular to the current direction did have a great impact on the $I_{\rm G}$ - $V_{\rm G}$ characteristics as shown in Fig. 4. It is considered to be due to the electric field concentration at SiO₂/SiC interfaces. Time-dependent dielectric breakdown (TDDB) tests are now under investigation.

4. Conclusions

It is revealed that there was no correlation between the experimental RMS values and surface roughness scattering. On the other hand, the surface morphology was considered to affect the long-term device reliability.

References

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Small

AFM images

Large

10.0nm

Roughness

Fig. 1. Schematic image of trench structure and results of AFM analysis in channel region. (a)-(c) show AFM images of each sample, and (d)-(f) were the corresponding line profiles in parallel with current direction.



Fig. 2. Analysis of effective channel mobility based on the mobility model [1]. The mobility was calculated from $I_{\rm D}$ - $V_{\rm G}$ characteristics measured at (a) -40, (b) 25, (c) 150, (d) 250° C.





Fig. 3. Characteristics of the effective mobility calculated from $I_{\rm D}$ - $V_{\rm G}$ curves with different RMS values as shown in Figs. 1(d)-(f).

Fig. 4. $I_{\rm G}$ - $V_{\rm G}$ characteristics. The corresponding AFM images and RMS values of line profiles which were perpendicular and parallel to the current direction were also shown.