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Characterization of Ga_2O_3 MOSFETs for Low to Medium Power Applications

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Abstract

As a contender for power electronics applications, β-Ga_2O_3 is well suited for unipolar, lateral device applications due to low dc conduction losses. However, to date, little work has been done to show dynamic switch loss potential. In this work, we establish an upper bound for dynamic switch loss metrics for current generation depletion and enhancement-mode β-Ga_2O_3 MOSFETs through C-V characterization. $R_{ON} Q_G$ values around 5200 mΩ-nC were measured on unoptimized enhancement-mode devices with three terminal breakdown voltage of 147 V. However, we project $R_{ON} Q_G$ values as low as 110 mΩ-nC by implementing realized ohmic contact optimization and scaling of parasitic access resistance. Further reduction is possible through materials optimization and device design.

1. Introduction

β-Ga_2O_3 has recently emerged as the only power semiconductor with a larger bandgap than GaN and SiC that offers large-area, native substrates grown from a melt and has achieved residual doping in epitaxial films as low as ~1E13 cm^{-3} to over 1E20 cm^{-3} for degenerately doped films [1]. Several groups have demonstrated high-quality, low-defect epitaxy by various growth techniques [2-5]. The critical field strength (E_C) of β-Ga_2O_3 is estimated to be ~8 MV/cm—about 2.5x that of bulk GaN and SiC. A key milestone was the empirical demonstration of record-high E_C > 3.8 MV/cm in a laterally scaled β-Ga_2O_3 MOSFET which is the first to surpass bulk GaN and SiC values [6]. While this device was not optimized for low on-resistance (R_{ON}), it clearly illustrated the strength behind lateral β-Ga_2O_3 MOSFET scaling of device geometry (including gate length) towards achieving lower R_{ON} and lower gate charge (Q_G). This high E_C affords tremendous opportunity for parasitic reduction that benefits both dc conduction losses and dynamic switch losses for power switching applications as well as high power-frequency product for RF applications.

To date, preliminary β-Ga_2O_3 devices have achieved > 600 V Schottky barrier diodes [7], 755 V breakdown in field-plated lateral FETs [8], > 600 V e-mode operation in wrap-gate FETs [9], and now GHz RF performance in MOSFETs [10]. Recent emphasis has been toward high-voltage commercial applications. However, there is a role for low- to medium-power applications in the 100's of Volts and 10's of Watts range with high switching speeds. Here, we provide early insight into the upper bound of dynamic switching losses through I-V and C-V characterization of short-periphery β-Ga_2O_3 MOSFETs grown homoepitaxially by two sources.

2. Device Fabrication

β-Ga_2O_3 MOSFETs were fabricated on 200-nm channels grown homoepitaxially by MBE with either Si [5] or Ge doping [4, 11]. Two-finger MOSFETs were made with 2 x 50 μm gate width with varying source-drain spacing (L_{SD}) and gate length (L_G). For both samples, electron mobility (μ) exceeding 100 cm^2/Vs was measured using on-wafer Van der Pauw test structures with moderate doping concentration varying in the range of 2-6E17 cm^{-3}. The contact resistance (R_C) was not optimized and resulted in about ~20 Ωmm or higher which can be drastically improved by implant ionization [7] or regrowth. For the Si-doped sample, a recess gate step was included to remove ~70% of the ~1 μm gated channel to render it normally-off which is a desired feature for fail-safe power switch devices. The Ge-doped sample was depletion-mode with L_G = 2 μm. A schematic of both devices and their geometry is illustrated in Fig. 1. Additional processing details can be found in prior reports [10, 11].

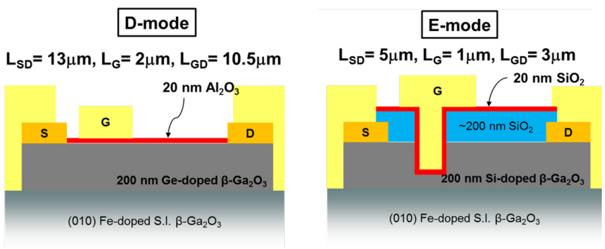

Fig. 1: (left) Ge-doped d-mode and (right) Si-doped e-mode β-Ga_2O_3 MOSFETs.

3. Device Characterization

Fig. 2 compares the family of output curves of representative d- and e-mode β-Ga_2O_3 MOSFETs where the maximum current reaches about 30 mA/mm at V_{DS}= 10 V. The d-mode device was optimized for higher breakdown (L_{SD} = 13 μm, L_G = 2 μm, L_{GS} = 0.5 μm, R_{SH} ~ 12 kΩ/sq) while the e-mode device was optimized for R_{ON} (L_{SD}= 5 μm, L_{GS} = L_G= 1 μm, R_{SH} ~ 6 kΩ/sq). Indeed, the breakdown voltage (V_{BK}) was 479 V and 147 V for the d-mode and e-mode devices, respectively. The V_{BK} of 479 V is close to the predicted maximum value using a peak E_C = 8 MV/cm according to the relationship, $V_{BK} = \varepsilon E_C^2/(2qN_D)$, predicted by Baliga for a doping concentration of ~4E17 cm-3. For the e-mode device, the R_{ON} was about ~180 Ω–mm at V_{GS} = 8 V.

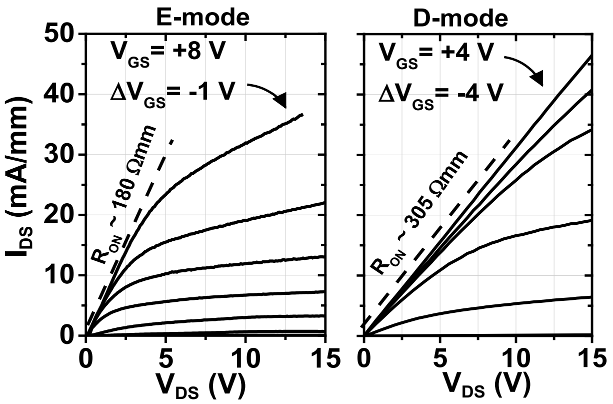

Fig. 2: I-V output curves for e-mode (left) and d-mode (right) β-Ga_2O_3 MOSFETs.

From C-V, we extract an upper bound for total gate charge, Q_G, by integrating C_G from $V_{G\text{-OFF}}$ to $V_{G\text{-}ON}$ for measured R_{ON} with V_{DS} = 0 V and use this to establish an upper bound for $R_{ON}\,Q_G = L_{CH}^2/\mu$ based on methods outlined by Schuette *et* al. [12]. The C-V characteristics measured at the device level are shown in Fig. 3. The e-mode MOSFET has lower Q_G because of the smaller L_G and gate recess. Figure 4 shows $R_{ON}\,Q_G$ as a function of V_{BK} computed from L_{CH}^2/μ with reference lines drawn for Si, GaN and β-Ga_2O_3. State-of-the-art Si and GaN devices are shown for reference [13, 14]. As a comparison, measured data for early generation d- and e-mode β-Ga_2O_3 MOSFETs shown as open dots are approaching state of the art Si trench MOSFETs. Simple optimization steps are calculated and shown as closed dots for each device based on known realizable improvements. First ohmic contact resistance is assumed < 0.2 Ω-mm. Second, we assume self-aligned source contact and scale the drift region and gate length to the Baliga limit for the doping used. Finally, we incorporate modest mobility improvement according to upper limits calculated by Ma et al. [15] to project $R_{ON}\,Q_G$ values of 70 and 245 mΩ-nC for e- and d-mode FETs respectively. This competes with state-of-the-art GaN with the added benefit of cost-effective bulk substrates.

4. Conclusion

Early results on β-Ga_2O_3 FETs show great promise for low dynamic loss switches and thus high-speed switching for power applications. We anticipate, based on materials optimization and advanced fabrication techniques, that we can meet or exceed dynamic switch loss metrics in lateral GaN devices while exceeding dc conduction loss metrics via the superior BFOM achievable by β-Ga_2O_3.

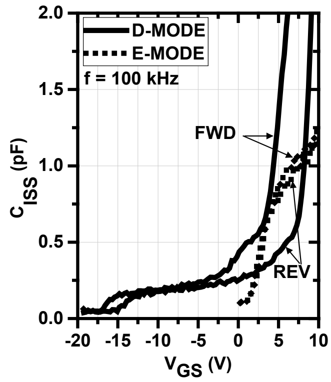

Fig. 3: Device C-V measurements for both e-mode and d-mode β-Ga_2O_3 MOSFETs.

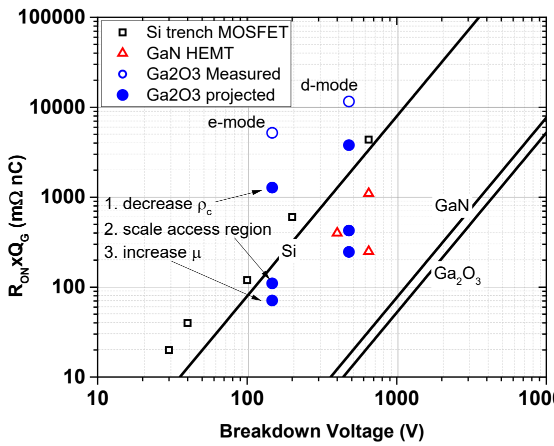

Fig.4: $R_{ON}Q_G$ vs V_{BK} plot showing unoptimized d- and e-mode β-Ga_2O_3 MOSFETs compared to state-of-the-art GaN and Si. A realistic resistance optimization path is shown by the solid blue circles.

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