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CMOS Readout Circuit with an On-chip Offset Voltage for Temperature Compensation of pH-ISFET Sensor

Ruey-Lue Wang[1], Cheng-Shiue Tsai[1], Kai-Bau Lee[1], Hui-Ya Chen[1], Yen-Yu Lin[1], Jhao-Yuan Chen[1], Yu-Ting Chuang[2], Hsin-Hao Liao[2], Hann-Huei Tsai[2] and Ying-Zong Juang[2]

[1] National Kaohsiung Normal Univ.
No.62, Shenjhong Rd., Yanchao District, Kaohsiung City 824, Taiwan (R.O.C.)
Phone: +886-7-7172930ext7916 E-mail: rlwang@nknu.edu.tw
[2] National Applied Research Laboratories, National Chip Implementation Center
7F, Chimei Builiding, Tzu-Chiang Campus, No.1, Ta-Hsuch Rd., Tainan City 701, Taiwan (R.O.C.)

Abstract

This paper presents a thermally stable CMOS pulse-width-modulation (PWM) readout circuit in which an offset voltage, V_{os}, is used for temperature compensation of the ion-sensitive field effect transistor (ISFET) of a pH sensor. The effective gate voltage, $V_{G,eff}$, of the ISFET in a phosphate-buffered saline (PBS) solution usually has a negative temperature coefficient. The V_{os} of the readout circuit is used to partially offset the input voltage, $V_{G,eff}$. The V_{os} can be chosen to be complementary to absolute temperature (CTAT) and hence the temperature drift of the $V_{G,eff}$ of the ISFET in a solution can be offset. The V_{os} comes from a multiple-positive-input operational amplifier in order that external or on-chip CTAT offset signals can be chosen. The variation quantity of the output pulse width with temperature is about 9.5 μs/°C and less than 0.5 μs/°C μs by using a constant and a CTAT offset voltage, respectively, over a temperature range from 10 to 50 °C.

1. Introduction

An extended-gate ion-sensitive field-effect transistor (ISFET) is a metal-oxide-semiconductor FET (MOSFET) with an extended top-metal gate electrode, on which a sensing film is coated. Under a bias voltage V_{ref} from a reference electrode such as Ag/AgCl, the H^+ ion concentration causes an corresponding interface potential on the sensing film that is measured as a change in the threshold voltage or a change in the effective floating-gate voltage, $V_{G,eff}$ [1, 2].

Several studies have demonstrated that ISFETs have large thermal instability due to characteristics of the sensing films [2-3], which results in inaccurate ion measurements. The temperature characteristics of ISFET sensors complexly depend on the reference electrode, electrolyte-insulator potential and ISFET-based MOS transistor. In this work, a CMOS pulse-width-modulation (PWM) readout circuit with an on-chip temperature-dependent offset voltage, V_{os}, is used for the temperature compensation of the ISFET of a pH sensor.

2. Sensing Readout Circuit Design

Fig.1 shows the circuit schematic of the PWM readout circuit with a V_{os} for temperature compensation of pH-ISFET [1]. The readout circuit consists of two voltage-to-current (V-I) converter, a comparator module, a charging and discharging module (CDM), an output module, and several current mirrors. The low-voltage cascoded current mirrors are used to mirror the charge, discharge, and offset currents to the CDM in order to charge or discharge the capacitor C_p. The transistor at the positive input terminal is an extended-gate ISFET. The native Al_2O_3 on the top metal is used as the sensing membrane. Its $V_{G,eff}$ acts as V_{sen}, and is converted into a current I_{sen}, i.e., $V_{SEN}/R1$, by one V-I converter. The current is used to generate a single pulse. Another V-I converter uses a multiple-input operational amplifier (OPA) with two positive inputs V_{dsg} and V_{os} to generate a discharge current I_{dag} or an offset current I_{os}, respectively. The I_{os} is used to offset the drift of $V_{G,eff}$ with temperature. By using the multi-input OPA, the circuits related to offset and discharge functions are combined. To facilitate the usage of various V_{os} voltage sources, another multiple-input OPA, which inputs come from an external voltage bias or outputs of an on-chip temperature sensors with multiple output voltages [4], is connected to the V_{os} terminal of the PWM readout circuit. The output of the OPA can be selected form these inputs by two selection signals. The temperature sensor mainly consists of three cascoded diode-connected sub-threshold NMOSFETs which V_{GS} decreases with increasing temperature under a bias current. Therefore, temperature characteristics of its drain voltages exhibit negative temperature coefficients (TCs) [4].

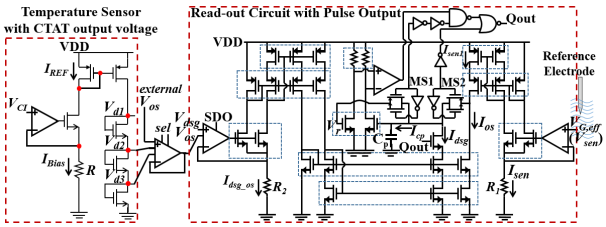

Fig. 1 Circuit schematic of the thermally stable CMOS PWM readout circuit with an on-chip offset voltage.

With two external signals RESET and SW, a specific control signal generator produces two control signals MS1 and MS2 to control transmission-gate (TG) switches of charging and discharging the capacitor Cp [1]. Initially, MS1 and MS2 are at the "0" and "1" levels, respectively, and the Cp is charged to have a voltage drop of V_r. When the signals MS1 and MS2 are at the "1" and "0" levels, respectively, the Cp is charged by the current $I_{cp}=I_{sen1}-I_{os}$ for a duration of one half-period of the SW. When the MS2 goes from low level to high level, the Qout also goes form low level to high level and

hence the Cp is discharged by the current I_{dsg} until its voltage drop V_{Cp} goes below the referred V_r. When the discharging of the Cp stops, the Qout goes from high level to low level immediately. By this procedure, a single pulse, which pulse width is linearly proportional to the V_{sen}, is generated at the Qout. The MS2 is also used to select V_{dsg} and V_{os} as the input of the multiple-input OPA. The circuit principle can be comprehended by referring to refs. [1]. The pulse width T_{pw} can be derived as follows.

$$(I_{sen1} - I_{os})(\frac{1}{2}T_{sw}) = I_{dsg}T_{pw} \quad (1)$$

$$T_{pw} = \frac{(V_{sen}/4R_1)-(V_{os}/4R_2)}{(V_{dsg}/16R_3)}(\frac{1}{2}T_{sw}) = \frac{2(V_{sen}-V_{os})}{V_{dsg}}T_{sw} \quad (2)$$

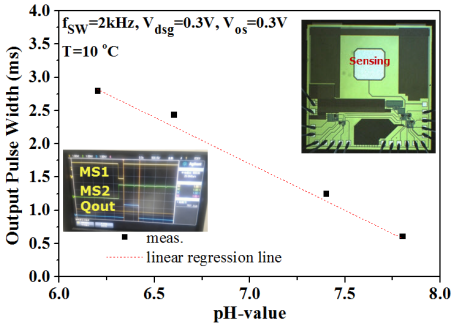

Fig. 2 Measurement result of the output pulse width related to the pH value of the analyzed solution.

Fig. 2 shows the measurement result of the output pulse width related to the pH value of the analyzed solution which is a phosphate-buffered saline (PBS) solution under a bias voltage V_{ref} of 1.5V, a V_{dsg} of 0.3V, and V_{os} of 0.3 V. The SW is a continuous pulse signal of 2 kHz. The inserted photographs are the measured waveform and the chip photograph of the readout circuit chip with a sensing area of 500×500 μm^2. The sensitivity is about -1.39 ms/pH with linearity of 99.36%.

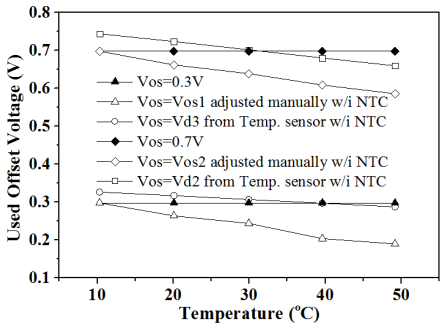

Fig. 3 Temperature characteristics of the used offset voltages for the PWM readout circuit.

Fig. 3 shows the temperature characteristics of the used offset voltages for the PWM readout circuit. These signals are the positive inputs of the multiple-input OPA and can be chosen as the output and then works as the V_{os} of the PWM readout circuit. 0.3V and 0.7V constant voltages, manually adjusted voltages with a specific negative TC, and the voltages coming from the output voltages of the on-chip temperature sensor are used as the V_{os}.

Fig. 4 shows the variation of the output T_{pw} with temperature under various offset voltages as shown in Fig. 3. The analyzed solution has a pH value of 6.6. With the constant offset voltages of 0.3 V or 0.7 V, the T_{pw} has a temperature coefficient of about -9.5 μs/°C. By using manually-setting CTAT V_{os} and on-chip CTAT V_{os} from V_{d2} with temperature coefficients of about -2.7 mV/°C and -2.1 mV/°C, respectively, the variations of the output pulse widths are about 0.15 μs/°C and -0.5 μs/°C, respectively, over a temperature range from 10 to 50 °C. This means that the variation of the $V_{G,eff}$ is about -2.7mV/°C. The temperature dependence of the T_{pw} is significantly improved by using a specific CTAT offset voltage. A higher voltage level of V_{os} can shift the T_{pw} to a lower value.

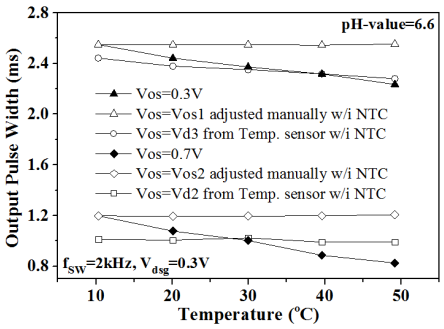

Fig. 4 Variation of the output pulse width with temperature under external constant and on-chip or external manually-setting CTAT offset voltages, respectively, for a PBS solution of pH value of 6.6.

3. Conclusions

A CMOS thermally stable PWM readout circuit for pH-ISFET sensors has successfully been designed and fabricated by the TSMC 0.18 μm process. The current consumption is about 0.26 mA under the supply voltage of 1.8 V. The circuit operates under a procedure of charging of fixed time and then discharging of fixed current. Two matched V-I convertors make the output characteristics of readout circuit itself thermally stable. In a solution with a pH value of 6.6, the variation of the effective input voltage, $V_{G,eff}$, is about -2.7mV/°C. A suitable CTAT V_{os} can be used to effectively reduce the temperature dependence of the output pulse width related to H^+ ion concentration in a solution. The sensitivity of the on-chip temperature sensor is -2.1mV/°C. Hence the sensor provides a slightly weak temperature compensation effect. But the on-chip offset voltage still provides a good temperature compensation. The equivalent drift of pH value is less than 0.0004/°C.

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