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Reliability Characteristics for Magnetic Tunnel Junctions with MgO Tunnel Barrier in Low Voltage

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Abstract

We investigated time-dependent dielectric breakdown (TDDB) modeling for MgO based magnetic tunnel junctions (MTJs) in low voltage by constant voltage stress (CVS) test. When electrons pass through the suppressed interface rather than the interface where trap sites are generated, a power-law V model should be applied. Even at low voltage of 1 V or less, it was confirmed that the TDDB experimental data and fitting of theoretical curve of the power-law V model show an error rate about 2.5 % when viewed as a voltage.

1. Introduction

MTJ consisting two ferromagnetic electrodes and a tunnel barrier between the electrodes have been intensively investigated for applications of read heads of hard disc drives and memory cells of magnetic random access memories (MRAMs) [1][2]. Nowadays, MTJs with a crystalline MgO as tunnel barriers and CoFeB as electrodes were commonly used to obtain high tunnel magnetoresistance (TMR) ratios [3]. Size of the MTJ must be reduced to achieve spin transfer torque (STT) operation. As the thickness of the tunnel barrier also becomes ultra-thin to 1 nm, the reliability studies of the fitting with the theoretical modeling curve, such as self-heating effect in the MTJ, E model, 1/E model and power-law V model, are underway. [4]. Previous work has shown reliability characteristics of the MTJ with Mg layer inserted to improve the interface between the MgO tunnel barrier and CoFeB [4]. Experiments have shown that the formation of trap sites varies depending on direction in which the electrons pass [5]. In this paper, we tried fitting TDDB with the theoretical curve when the Mg layer was inserted and the trap sites were suppressed. TDDB, which was studied only at a high electric field (> 10 MV/cm) or voltage (> 1 V). In this study, we measured TDDB at a lower electric field or voltage, and the study was conducted to fit it with the theoretical modeling curve.

2. General Instructions

Device fabrication

To evaluate TDDB characteristics for MTJs in low voltage, we fabricated MTJ structures with an Mg layer inserted below the MgO dielectric. We deposited multilayer stacks on thermally oxidized Si substrates by using an ultrahigh vacuum magnetron sputtering system with a base pressure of less than 4×10^{-7} Pa. The stacks had the following structure, with numbers in parentheses representing thicknesses in nm: Ta (5) /Ru (10) /Ta (5) /$Ni_{80}Fe_{20}$ (5) buffer layer /$Ir_{20}Mn_{80}$ (11) /$Co_{75}Fe_{25}$ (CoFe) (2.5)/ Ru (0.85)/ $Co_{40}Fe_{40}B_{20}$ (CoFeB) (2) /CoFe (1) /Mg (0.25 or 0.5) /MgO (1) /CoFe (0.4) /CoFeB (2) /Ta (2) /Ru (8). Here, the CoFe layers below the Mg insertion and above the MgO layer are inserted to promote crystallization of the CoFeB layers for a large TMR ratio. After deposition, the stacks were annealed at 360 ℃ for 30 min under a 5 kOe magnetic field to obtain a large TMR ratio and to improve magnetic hysteresis. The stacks were then patterned into 100 × 200 nm^2 ellipsoidal shapes by means of electron beam lithography, photolithography, and Ar-ion milling. Fig. 1 is a cross-sectional schematic of the MTJ.

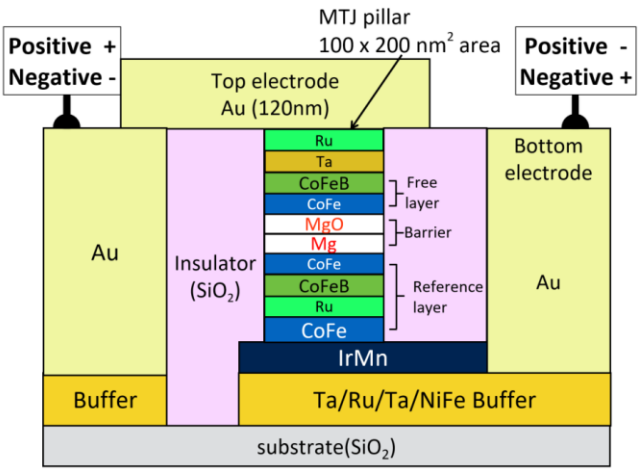

Fig. 1 Cross-sectional schematic of a MTJ device.

Power-law V model

Fig. 1, it is confirmed that the Mg layer is inserted under the MgO tunnel barrier. In other words, the roughness of the MgO bottom interface is improved to suppress the formation of trap sites [6]. We try to fit the power-law model. This is because, in the case of 1/E model with trap sites suppressed, TDDB rises very steeply in the low electric field, so that the error rate is considerably larger than the actual TDDB value. In the power-law voltage V model (power-law V model), failure of a dielectric layer is scaled by an applied voltage instead

of an electric field, and this model is appropriate for evaluating the reliability of an ultra-thin (< a few nm) dielectric [4][7]. The reason why a voltage instead of an electric field is used in this model is that it is expected that electron tunneling can occur without any energy (eV) loss due to dominance of ballistic transport in ultra-thin dielectric cases. T_{BD} (Breakdown time) in the power-law model can be written as the following equations (1), (2) [4][7]:

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$$T_{BD} = B_0(V)^{-n} \exp\left(\frac{Q}{k_B T}\right) \qquad (1)$$

$$n = -\left[\frac{\partial \ln(T_{BD})}{\partial \ln V}\right]_T \qquad (2)$$

where Q is the effective activation energy, B_0 is the process/material-dependent prefactor, k_B is the Boltzmann's constant, T is the absolute temperature, n is the power-law exponent. The key reliability physical parameters are the TDDB kinetic values (n and Q), which are determined from experimental TDDB data using the following equations:

Table I Physical parameters of the power-law V-model [4][8]

Symbol	Quantity	Parameter
Q	Effective activation energy	0.5 eV
k_B	Boltzmann's constant	$8.617 \cdot 10^{-5}$ eV·K^{-1}
n	Power-law exponent	100
B_0	Process/material-dependent prefactor	–1.5 ~ 1.0 (300~450 K)

ev = electronvolt

Experimental results

As shown Fig. 1, constant voltage stress (CVS) test was conducted at negative bias with electrons having the MgO/Mg interface as anode. Fig. 2, TDDB measurements below 0.8 V are still in progress as it is expected to take more than 10 million seconds (s) at 0.8 V or less. At room temperature, lower than 85 ℃, Since the model curve rises vertically about 10^2 ~ 10^3 s than Fig. 2, the temperature and voltage conditions that can be measured are set as above. TDDB measurement was conducted using the CVS test method. Fig. 2 graph shows the results obtained by applying the Weibull distribution and extracting TDDB data and fitting the data based on the breakdown of 63% MTJ under one condition, as in the previous work. At 0.9 V and above, 20 samples were broken down at each voltage condition. At 0.8 and 0.85, which are lower than 0.9 V, the breakdown time was very long. So, five MTJ breakdown data were extracted under each condition. Fig. 2 graph shows that the error rate between the model curve at less than 1 V and TDDB data is less than 2.5% at 0.8 V and in high voltage condition, the fitting is well. As a result, it can be confirmed that even if the interface where trap site generation is suppressed is an anode, it is fitting even at low voltage.

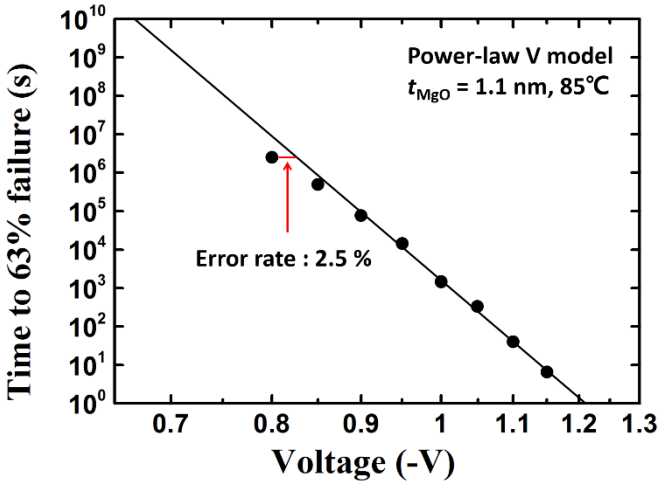

Fig. 2 Fitting graph of TDDB and power-law V model curves measured at t_{MgO} = 1.1nm, 85℃ and negative bias.

3. Conclusions

In this paper, we confirmed that a power-law V model should be applied when electrons pass through the interface where trap sites are suppressed. The voltage error ratio of the fitting between TDDB and power-law V model at low voltage was about 2.5% at the greatest, and it was confirmed that power-law V model was applicable at low voltage. In future, it should be studied whether the power-law V model can continue to be applied when electrons pass by setting the interface where the trap sites are generated to the anode. In addition to DC stress conditions, reliability studies should be continued under continuously switched AC stress conditions.

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References

[1] M. Durlam *et al*., *Electron Devices Meeting, IEDM '03 Technical Digest* (2003) 34.6.1.

[2] M. Hosomi *et al*., *Electron Devices Meeting, IEDM '05 Technical Digest* (2005) 459.

[3] C. Yoshida *et al*., *2009 IEEE International Reliability Physics Symposium* (2009) 139.

[4] C. M. Choi *et al*., *Semiconductor Science and Technology* **31** (2016) 075004

[5] C. M. Choi *et al*., *Electronics Letters* **52** (2016) 531

[6] C. M. Choi *et al*., *Electronics Letters* **52** (2016) 1037

[7] J. W. Mcpherson *Reliability Physics and Engineering 2nd ed.* (2013) 161

[8] E. Y. Wu *et al*., *Microelectronics Reliability* **45** (2005) 1809