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Fabrication of a Si Nanowire MOS Capacitor for the Application to Energy Storage Devices

Ryota Nezasa,Yasuyoshi Kurokawa, and Noritaka Usami

Nagoya Univ.
Furo-cho, Chikusa-ku, Nagoya 464-8603, Japan
Tel: +81-52-789-3246, Fax: +81-52-789-4516, E-mail: nezasa.ryouta@d.mbox.nagoya-u.ac.jp

Abstract

The capacitors using Si nanowires (SiNWs) prepared by metal assisted chemical etching (MACE) were fabricated for more simple processes and electronic characteristics were measured for the application to energy storage devices. The capacitance density of the capacitor using 3.0μm SiNWs at *V* = -6 V, *f* = 1 kHz was about three times higher than that of the planar ones. That means the capacitors using MACE-SiNWs can obtain a large capacitance using simple processes.

1. Introduction

Electrostatic capacitors are one of energy storage devices. They have considerably higher power densities than batteries and electrochemical capacitor because of their high charge/discharge rates [1]. Moreover, electrostatic capacitors have high mechanical and thermal stabilities [1]. These characteristics of electrostatic capacitors are attractive for application to energy storage devices. However, the electrostatic capacitors have considerably lower energy densities than batteries and electrochemical capacitors. Thus, it is needed to develop electrostatic capacitors with higher capacitance density.

Capacitance of a planar electrostatic capacitor is given by the following equation.

$$C = \varepsilon S/d \quad , \ldots (1)$$

ε is the dielectric constant of the oxide layer, S is the electrode surface area, and d is the oxide layer thickness. Therefore, the capacitance can be increased by optimizing these three parameters. In this experiment, we focused on S, and adopted 3-dimentional (3-D) structures to obtain a large effective surface area. Silicon nanowires (SiNWs) are one of the 3-D structures and have a large effective surface area. They have applied to several electronic devices, for example, transistors [2], solar cells [3] and MOS capacitors [4]. It has been reported that a capacitance density of 18 μF/cm^2 using SiNWs with 10-nm-thick Al_2O_3 thin film [4] were obtained. However, the SiNWs were fabricated using chemical vapor deposition that requires high temperature (425 ^{o}C ~) and vacuum technology. Thus, the process costs high and is not simple. Metal assisted chemical etching (MACE) is one of the fabrication methods of SiNWs [5]. The process is simple and no vacuum technology. Large effective surface area can be obtained easily at low cost. However, there are few reports on capacitors using SiNWs prepared by MACE (MACE-SiNWs) [6]. In this study, we fabricated capacitors using MACE-SiNWs. The Al_2O_3 thin film fabricated by the atomic layer deposition (ALD) method was used as the dielectric layer because ALD is effective for preparing thin films on structures with a high aspect ratio. Capacitance-voltage (*C*-*V*) and leakage current density-Voltage (*J*-*V*) characteristics were measured to evaluate qualities of the capacitors.

2. Experimental

Figure 1 shows a schematic diagram of a SiNW MOS capacitor fabricated in this experiment. p-type Cz-Si (100) wafers, which have 500±25 μm thickness and resistivity of 2-5 Ω・cm, were used. First, SiNWs were prepared on the Si wafers by the MACE method. The Si wafers were dipped in the $AgNO_3$ and HF mixed solution ($AgNO_3$: HF : H_2O = 120 mg : 10 mL : 40 mL) for 50 seconds to deposit Ag nanoparticles. After that, the Si wafers with the Ag nanoparticles were dipped in the H_2O_2 and HF mixed solution (H_2O_2 : HF : H_2O = 0.7 mL : 10 mL : 40 mL) to etch Si using the Ag nanoparticles as catalysts. The samples were immersed in HNO_3 for 10 minutes and HF (5%) for 1 minute to remove Ag residues for three successive cycles. Before the Al_2O_3 dielectric thin film deposition on SiNWs, the samples were cleaned by dipping in a piranha solution at 120~140 ^{o}C for 15 minutes and HF (5%) at room temperature for 1 minute. The Al_2O_3 thin film was deposited on SiNWs by ALD at 200^{o}C, in 200 cycles using $Al(CH_3)_3$ and H_2O as precursors. The nominal thickness of the Al_2O_3 dielectric thin film is about 20 nm. After that, the samples were annealed at 400 ^{o}C for 30 minutes in a forming gas (Ar:H_2 = 97:3) atmosphere to improve the quality of the thin film. Al was deposited on Al_2O_3/SiNWs surface by vacuum evaporation method as a surface electrode. The size of the

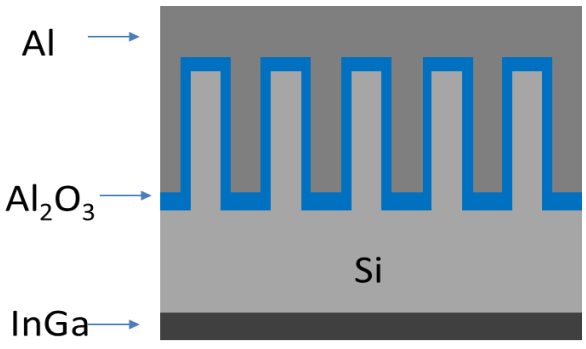

Fig. 1 Schematic diagram of a SiNW MOS capacitor.

electrodes was 0.5 mmϕ. InGa was pasted on the back surface as a back electrode. The structure of the samples was characterized by scanning electron microscopy (JEOL. JSM-7001FA). *C-V* and *J-V* characteristics were also measured using LCR meter and electrometer, respectively.

3. Results and discussion

Figure 2 (a1) and (b1) show cross-sectional SEM images of SiNWs after depositing the Al_2O_3 thin film. Etching duration during the MACE is (a1) 2 and (b1) 5 minutes. The average lengths of SiNWs etched for 2 and 5 minutes were 1.4 and 3.0 μm, respectively. Figure 2 (a2) and (b2) show the cross-sectional SEM images of the SiNWs after depositing the Al electrode. It is found that there are differences of the state of Al between the top and bottom of SiNWs. From EDS mapping, signal from Al was weaker at the bottom region than the top region, suggesting that Al coverage is not enough at the bottom region.

Figure 3 (a) shows *C-V* characteristics of the capacitors using the flat wafer and SiNWs with the length of 1.4 and 3.0 μm. The capacitance of 0.995 μF/cm^2 was successfully obtained in the case of SiNWs with the length of 3.0 μm at f = 1 kHz, V = -6 V. This value was about three times higher than that of the planar sample. This suggests the large effective surface area of SiNWs increased a capacitance density. The capacitance density of the capacitors using SiNWs became higher as the length of SiNWs got longer. It is because an Al coverage area is larger in the case of the longer SiNWs from SEM images and EDS mappings. However, the capacitance densities were lower than the ideal one we calculated. It is because Al was not fully covered on the whole of SiNWs. If the perfect coverage of the Al electrode is obtained, higher capacitance density can be expected. The large frequency dispersion at accumulation was also observed on the samples using SiNW and the frequency dispersion became larger as the length of SiNWs got longer. One of the reasons is due to high density of surface defects on SiNWs. It has been reported that SiNWs prepared by MACE using Si wafers with low resistivity (0.005 Ω·cm) have porous structure on the surface [7]. This suggests chemical etching using oxidation-reduction reaction may cause structural defects on the surface. Therefore, it is necessary to reduce surface defects before depositing Al_2O_3 to obtain capacitors with higher quality.

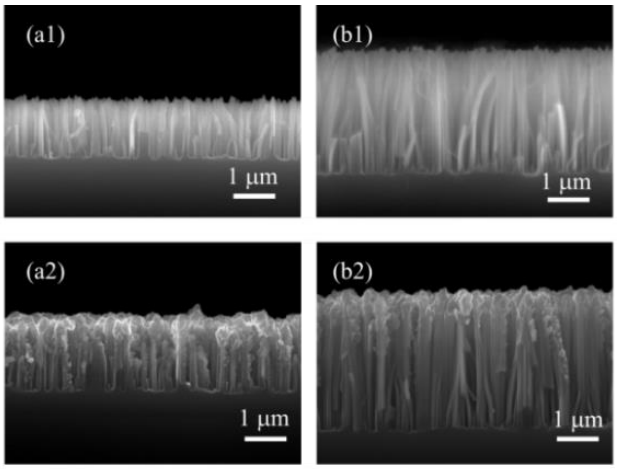

Fig. 2 Cross-sectional SEM images of SiNWs (a1, b1) after depositing Al_2O_3 and (a2, b2) after depositing Al. Etching duration during MACE is (a1, a2) 2 minutes and (b1, b2) 5 minutes.

Figure 3 (b) shows *J-V* characteristics of the capacitors using the flat wafer and SiNWs. The leakage current density of capacitors using SiNWs was higher than that of the planar capacitor, and increased with the length of SiNWs. It is because there are many defects on the Al_2O_3/SiNWs interface. To reduce leakage current density, surface defects at the interface of Al_2O_3/SiNWs should be reduced further.

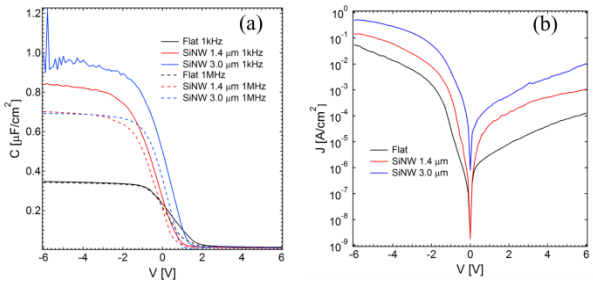

Fig. 3 (a) *C-V* curve, (b) *J-V* curve of SiNW MOS capacitors with different lengths of SiNWs.

4. Conclusions

The MOS capacitors using SiNWs prepared by the MACE method were fabricated and the electronic characteristics were evaluated. The average SiNWs length of 1.4 and 3.0 μm were obtained by the etching for 2 and 5 minutes, respectively. The capacitance density of 0.995 μF/cm^2 at V = -6 V, f = 1 kHz were successfully obtained in the SiNWs with the length of 3.0 μm. That was about 3 times higher than that of the planar capacitor. The high capacitance density is due to a large effective surface area of SiNWs. The capacitance of the samples using SiNWs are lower than calculated value due to low coverage of the Al electrode. If the perfect coverage of the Al electrode is obtained, higher capacitance density can be expected.

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