Fabrication of Gate-All-Around Poly-Si Tube-channel Junctionless Field-Effect Transistors

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Abstract

We reported a novel process for the successful demonstration of junctionless poly-Si field-effect transistors (FETs) with an ultra-thin tube channel and gate-all-around configuration. The fabricated devices show well-behaved performance with on/off current ratio greater than \(10^7\) and subthreshold swing of 98 mV/decade. We also show that parasitic effects arising from the underneath channel can be effectively suppressed by using a substrate implant design.

1. Introduction

Macaroni FETs have been aggressively employed in the construction of 3D NAND flash memories [1]. This scheme features an ultra-thin tube-shaped poly-Si channel, within which an oxide layer is filled into the core of the tube channel in order to avoid the degradation in subthreshold swing that occurs to the devices with a thick cylindrical channel. In view of the exquisite combination of ultra-thin channel and gate-all-around (GAA) configuration [2], the macaroni-channel FET provides promising potential for relieving short-channel effects encountered for sub-micrometer-scale and even nanometer-scale CMOSFETs, despite the fact that few works have been reported on the subject. In this abstract, we presented a new, novel process for the fabrication of GAA poly-Si FET with a tube-shaped channel.

2. Experiment

Cross-sectional and plan-view structures of the Tube-FET, are sketched in Fig. 1. Apart from the Macaroni FETs, the tube-channel conformally encapsulating a dielectric core is horizontally lying between source and drain (S/D) studs. Figure 2 illustrates the process flow of the Tube-FET. The fabrication began with a Si substrate that was intentionally implanted with B⁺ in order to suppress the leakage of the parasitic transistor (Fig. 3) is evidenced in Fig. 6. Two test devices (specified with symbols) with and without implantation, respectively, were fabricated by similar process flow shown in Fig. 2, except that the formation of the core channel is skipped. For comparison, I-V curve of the Tube-FET shown in Fig. 5 is also included in the figure (the dashed line). Transfer characteristics of test devices without implant in Fig. 6 suggest that the deposition of heavily doped poly-Si on the Si substrate would become a leak path, resulting leakage current much higher than that conducting through the tube poly-Si channel. This issue can be resolved by conducting counter implant doping. As shown in Figure 5, the leakage current of the parasitic transistor is well suppressed to a level that is much lower than that of the Tube-FET as the substrate implant was performed.

3. Results and discussion

The cross-sectional TEM image of a fabricated device is shown in Fig. 4, in which there appear conformal layers of poly-Si channel and oxide encapsulating the nitride core. The perimeter of the core represents the effective channel width of the devices, and the estimated channel width for our device is approximate 330 nm from TEM observations. The transfer characteristics of the Tube-FET with L/W of 110nm/350 nm are displayed in Fig. 5. It is clearly seen that well-behaved switching performance withIon/Ioff current ratio greater than \(10^7\) is achievable for the Tube-FET. Moreover, despite the high doping concentration of the channel layer, a good subthreshold swing of 98 mV/decade is measured, thanks to the ultra-thin tube channel and GAA configuration.

Effect of the ground-plane (substrate) implantation for suppressing the leakage of the parasitic transistor (Fig. 3) is evidenced in Fig. 6. Two test devices (specified with symbols) with and without implantation, respectively, were fabricated by similar process flow shown in Fig. 2, except that the formation of the core channel is skipped. For comparison, I-V curve of the Tube-FET shown in Fig. 5 is also included in the figure (the dashed line). Transfer characteristics of test devices without implant in Fig. 6 suggest that the deposition of heavily doped poly-Si on the Si substrate would become a leak path, resulting leakage current much higher than that conducting through the tube poly-Si channel. This issue can be resolved by conducting counter implant doping. As shown in Figure 6, the leakage current of the parasitic transistor is well suppressed to a level that is much lower than that of the Tube-FET as the substrate implant was performed.

4. Conclusions

A new junctionless Tube-FET process was demonstrated in this work. The combination of ultra-thin tube channel and GAA configuration enables good switching performance even though the junctionless scheme with a highly doped channel is employed. We also showed that the influence of a parasitic transistor can be effectively suppressed by a ground-plane implant.
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**References**