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Detection of electron trapping/detrapping in MoS_2 FET by high time-resolved I-V measurement

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Abstract: For exploring the origin for the interface states in MoS_2 FET, the transient response of MOS capacitor to ultra-fast pulsed top gate voltage was studied with high time resolution current measurement system. The difference of time constant originated from trapping and detrapping of electrons on interface states was detected, which cannot be measured in C-V measurement.

1. Introduction

MoS_2 field-effect transistors (FETs) with high-*k* oxides have attracted much attention as a potential candidate for the scaled electron device application because its atomically thin layers are able to suppress short channel effects. The understanding of the interfacial properties between 3-dimensional oxide and 2-dimensional layered channel is the key to improve the gate controllability. Recently, for MoS_2 FET, interface states density (D_{it}) and its time constant (τ_{it}) are estimated to be ~10^{13} $cm^{-2}eV^{-1}$ and the order of μs near the conduction band edge, respectively, based on both subthreshold swing (S.S.) of current-voltage (*I*-*V*) curve and capacitance-voltage (*C*-*V*) analysis [1]. However, D_{it} values are largely scattered from ~10^{11} ~ 10^{13} $cm^{-2}eV^{-1}$, depending on the sample quality and measurement methods [2,3]. Therefore, the transfer characteristics reported so far in many papers are largely degraded from the ideal due to the electron trapping to the interface states. To evaluate the effects of electron trapping and understand the origin for the interface states, the multi-facetted investigation is necessary.

In this paper, high time-resolved *I*-*V* measurement with the maximum time resolution of 10 ns, which is shorter than τ_{it}, is employed to probe current-time evolution caused by trapping/detrapping response of electrons to the interface states.

2. Device fabrication

Monolayer MoS_2 films were transferred on a quartz substrate from natural bulk MoS_2 flakes. Ni/Au were deposited as source/drain electrodes. Then, Y metal with the thickness of 1 nm was deposited as a buffer layer with the thermal evaporation in Ar atmosphere of 10^{-1} Pa, followed by laboratory air oxidization. The top gate Al_2O_3 insulator with the thickness of 10 nm was deposited by atomic layer deposition. Finally, Al/Au were deposited as the top gate electrode. **Fig. 1** shows the schematic of the device structure and its optical images. The high time-resolved *I*-*V* measurement was carried out using Agilent B1530.

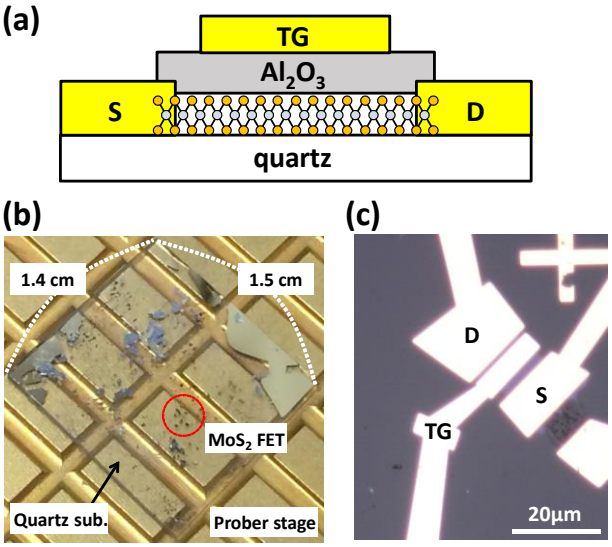

Fig. 1 (a) schematic of monolayer MoS_2 FET on quartz substrate. (b) Optical image of the quartz substrate. (c) Optical image of magnified MoS_2 device.

3. DC *I*-*V* measurement

First, DC *I*-*V* measurement was performed to estimate D_{it} of the MoS_2 FET device by the S.S. analysis. **Fig. 2** shows I_d-V_{TG} with the current on/off ratio over 10^6. With the help of the top gate oxide capacitance (C_{ox}) determined by the *C*-*V* measurement, D_{it} dispersion near conduction band edge was extracted, as shown in the inset of **Fig. 2**.

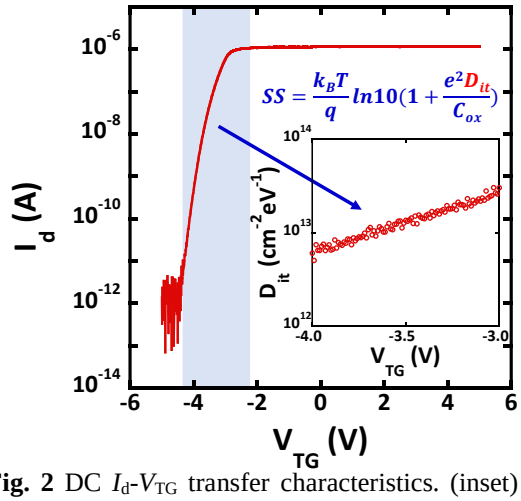

Fig. 2 DC I_d-V_{TG} transfer characteristics. (inset) D_{it} near the conduction band edge as a function of V_{TG}.

The value of ~10^{13} $cm^{-2}eV^{-1}$ for D_{it} is suggested to be large enough to detect the effect of electron trapping to the interface states by high time-resolved *I-V* measurement.

4. high time-resolved capacitance measurement

The ultra-short voltage pulse was applied to the top gate and time response of I_d was measured with the time resolution of 10 ns, as shown in **Fig. 3(a)**. This is the simple MOS capacitance measurement. The equivalent circuit is shown in **Fig. 3(b)**, where the interface trap capacitance and resistance (C_{it} & R_{it}) are included with the quantum capacitance (C_Q) of monolayer MoS_2. Therefore, the effect of electron trapping to the interface states can be extracted by analyzing the transient response to the ultra-short V_{TG} pulse.

Experimentally, there are two important issues. One is parasitic capacitance (C_{para}) between metallic substrate and the probe pads with quite large area compared with the channel area, because MoS_2 FET is generally fabricated on the highly-doped Si substrates. Therefore, the MoS_2 FET were prepared on quartz substrate in order to remove the contribution of C_{para} in this study. The other is the issue on the voltage reflection due to the long transmission line, since the short voltage pulse is composed of high frequency sine waves and the transmission line itself is often dealt as circuit elements. Therefore, the transmission line was prepared as short as possible.

Fig. 3(c) shows schematic of drain current response to top-gate voltage pulse (V_{TG}). In this experiment, maximum V_{TG} value (V_{fin}) was fixed at 5 V and initial voltage (V_{init}) was varied to reveal the dependence of initial Fermi level on transient response. Both rising time (t_R) and falling time (t_F) was selected as 500 ns. The top three figures in **Fig. 4** show absolute value of I_d as a function of time for both rising and falling sides at different V_{init}. It is evident that the transient behavior for rising and falling sides is different at V_{init} = -5 V. For other V_{init}, on the other hand, the

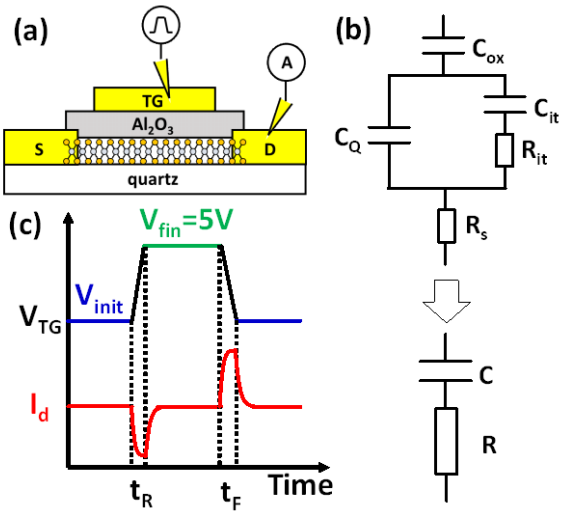

Fig. 3 (a) Schematic of measurement setup. (b) Equivalent circuit of measured system and simplified circuit. (c) Schematic of applied V_{TG} and expected I_d response.

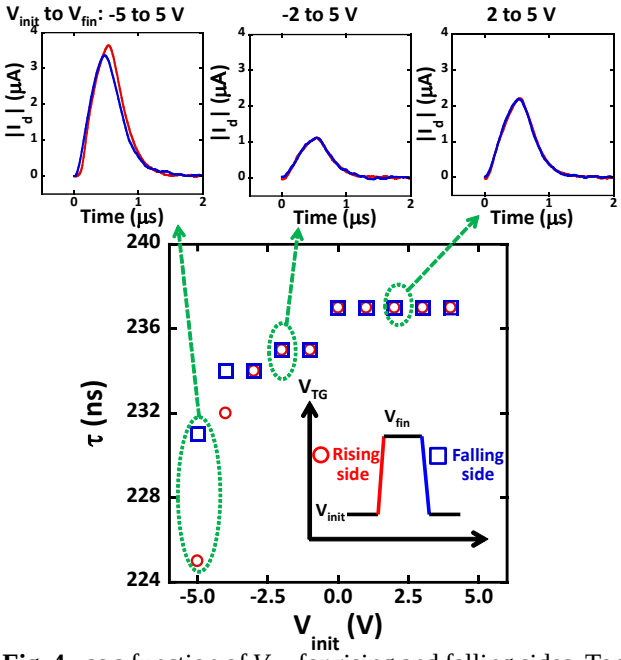

Fig. 4 τ as a function of V_{init} for rising and falling sides. Top three figures compares absolute value of I_d as a function of time for both rising and falling sides at different V_{init}.

difference cannot be seen. Here, the equivalent circuit is composed of only capacitors and resists, so this can be simplified as single RC circuit, as shown in **Fig. 3(b)**. Then, the time constant for single RC circuit (τ = RC) was evaluated by fitting the decay behavior of I_d for both rising and falling sides. These are plotted as a function of V_{init} in **Fig. 4**. With decreasing V_{init} from 4 V to -5 V, the difference in τ increases. As can be seen in **Fig. 2&3**, the contribution of C_{it} ($=e^2D_{it}$) to the total capacitance for monolayer MoS_2 is large at the subthreshold region. However, with increasing V_{init}, i.e., approaching to the conduction band edge, C_Q ($=e^2DOS$) for monolayer MoS_2 become dominant. Therefore, the difference in τ for rising and falling was observed only at V_{init} in the subthreshold region. Because the rising and falling sides correspond to trapping and detrapping of electrons, respectively, this difference indicates the difference in τ for trapping and detrapping. Generally, τ for trapping and detrapping cannot be separated in *C-V* measurement because of AC measurement. This is the advantage of ultra-fast pulse measurement.

5. Conclusions

The difference of time constant originated from trapping and detrapping of electrons on interface states was evaluated with high time resolved *I-V* measurement.

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