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Investigation of Transient Thermal Dissipation in Three-Dimensional Stacked ICs

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Abstract

Three dimensionally stacked ICs (3DS-ICs) is expected to be small footprint, energy efficient and high-functional due to its short chip-to-chip signal transfer distance by stacking thinned LSIs. At the same time, thermal characteristics degradation is concerned by increased thermal gradient on the LSIs with thinned base silicon. To manage this thermal environment in the 3DS-ICs, thermal characteristics of the thinned LSIs must be clarified. In this paper, static and dynamic thermal dissipations observed on both before and after thinning silicon for comparison. Measured results revealed silicon thinning affects both static and dynamic thermal characteristics. It suggests that dynamic heat dissipation should be analytically understood as well as static one, for reliability of 3DS-ICs.

1. Introduction

Three dimensional stacked ICs (3DS-ICs) is getting a lot of attention due to the end of device scaling. Thermal conductive base silicon (Si) must be highly thinned to manufacture through-silicon via for communication among tiers. Reduced heat conductivity of thin silicon makes large thermal gradient which leads degradation of circuit characteristics and even short lifetime according to Arrhenius law. To prevent these reliability issues, we need analytical understanding of thermal environment in 3DS-ICs.

Several researches discussed about maximum temperature and temperature rise time of a hotspot on LSI with thinned base Si [1] [2], they suggests that the relation between thermal characteristics and vertical interconnect distance is a trade-off relation. In this research, we manufactured a test vehicle with densely area-arrayed thermal sensors and switchable heaters for thermal characteristics evaluation with thinned base Si. We evaluate dynamic heat distribution as well as static one at hotspot and surrounding areas, and discuss about the thermal environment variation in 3DS-ICs.

2. CMOS test vehicle and test setup

The test vehicle shown in Fig. 1 is manufactured with 1.8 V V_{DD}, 130 nm CMOS process. As Fig. 2 shows, the test vehicle has arrayed heaters and sensors to investigate thermal distribution in various test situations. A 25 μm (20 μm Si, and 5 μm BEOL) thinned sample is assembled as Fig. 3 (a) as well as 725 μm thickness sample in Fig. 3 (b). For better handling, 200 μm thickness bare Si die is attached to thinned sample with low heat conductive die-attach-film to attenuate heat dissipation to the bare Si die. Both 25 and 725 μm samples are mounted on FR-4 board and molded with epoxy resin.

A measurement setup in this research is shown in Fig. 4.

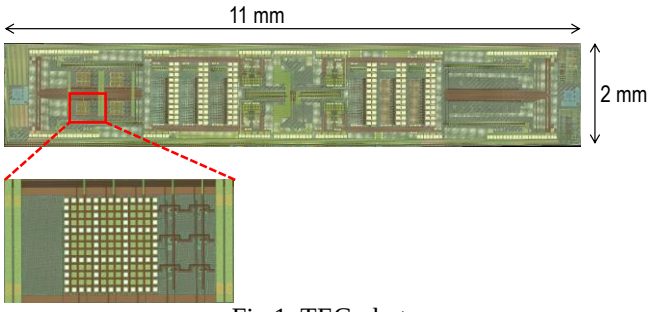

Fig.1. TEG photo.

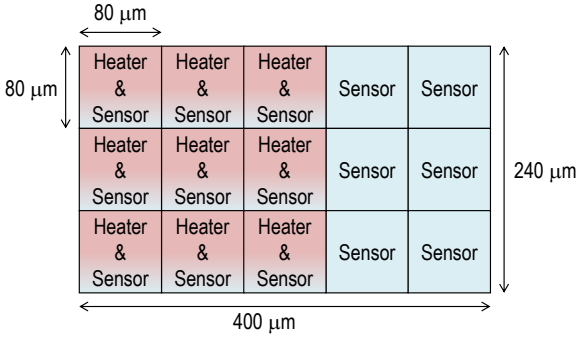

Fig.2. Test structure diagram.

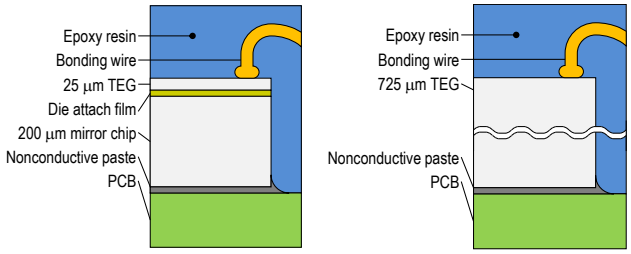

Fig.3. TEG assembly diagram of (a) 25 μm sample and (b) 725 μm sample.

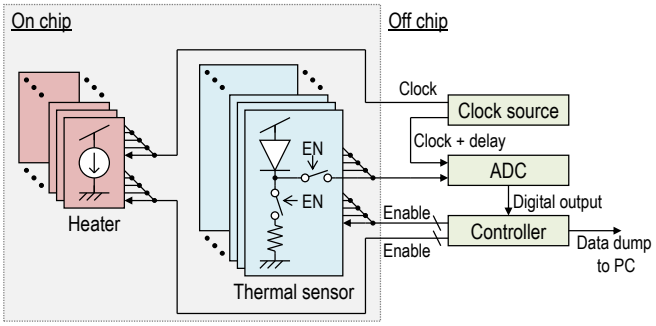

Fig.4. TEG evaluation setup.

Heater is selected by enable signal from controller, and activated while clock signal is high. Single sensor is selected from 15 areas and sensor output is digitized by ADC at the timing synchronized with the clock signal. Iterative acquisition of sensor output with ΔT delay provides dynamic

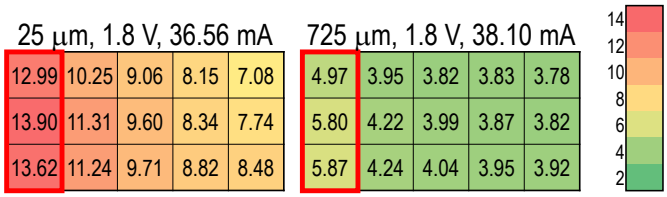

Fig.5. Measured static heat distribution map of 25 µm sample and 725 µm sample.

temperature distribution with timing resolution of ΔT. For static temperature distribution, clock signal is fixed high in this study.

3. Measured result

The static thermal distribution is evaluated and result is shown in Fig. 5. Left 3 heaters are activated and the values in the result are temperature variations from room temperature of 22 deg. C. We can see heat gradient around heater activation area indicated with red line, and the temperature highly depends on Si thickness. The result also shows tendency that bottoms area temperature are higher than top areas even test area layout is horizontal symmetry. This tendency is considered to be from smaller heat conductive Si area due to chip edge near bottom areas.

Fig. 6 shows the dynamic thermal variations evaluated with switching heaters with clock frequency of 5 kHz and duty cycle of 25 %. As shown in Fig. 6(a) Left 3 heaters are activated and temperatures on central 5 areas are measured and plotted. We can see large dynamic temperature variation and nearby area of the heaters has also dynamic variation in the case of 25 µm sample in Fig. 6(b). On the other hand, only one area has dynamic variation in the case of 725 µm sample in Fig. 6(c). This is considered to be from smaller heat capacity on base Si makes rapid heating of heater area and propagation to next area by larger temperature gap. In this research, we can see 28 µs delay between heater temperature peak and next area temperature peak, this is considered to be from large heat resistance and small heat capacity of the sample. An early stage thermal network analysis is done for this structure and shows similar dynamic temperature variations and heat propagation delay.

The evaluations demonstrated Thinning drastic change on both static and dynamic thermal distribution by thinning LSI. Thermal propagation delay is also shown and it suggests that better reliability of 3DS-ICs requires understanding of dynamic thermal characteristics.

4. Conclusions

Thinning LSI for 3DS-ICs integration is considered to cause thermal characteristics variation as well as electrical and mechanical ones. In this research, static and dynamic thermal distribution of thinned LSI is evaluated. The evaluation result shows higher thermal gradient of thinned sample in both static and dynamic thermal characteristics. In the dynamic heat propagation, temperature peak delay between heater and next area is observed. From these result,

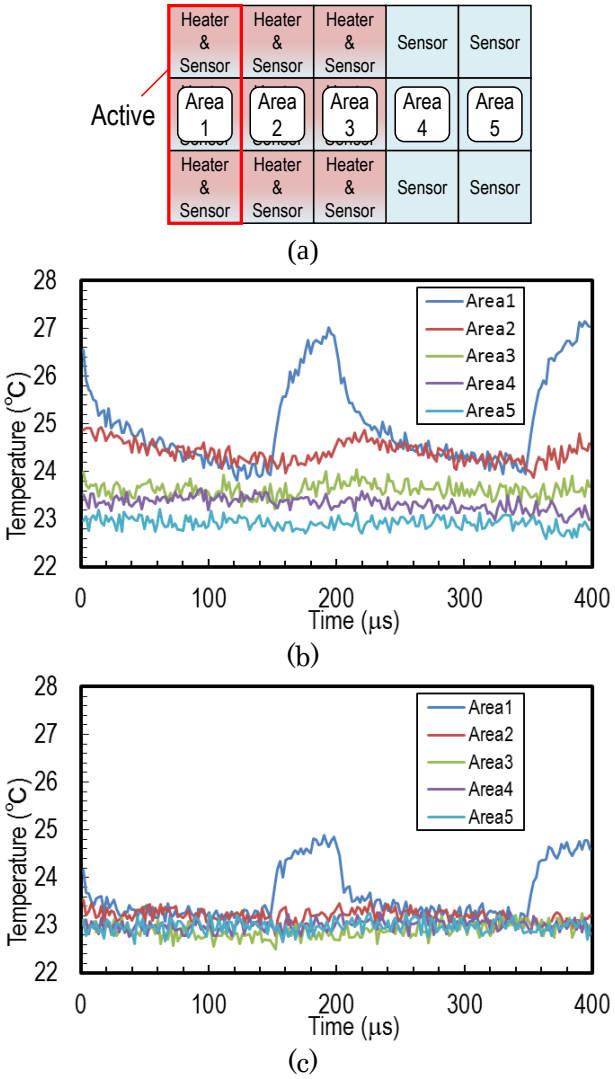

Fig.6. (a) Activated heaters and target area for dynamic temperature measurement. (b) Measured dynamic temperature plot of 25 µm sample and (c) 725 µm sample.

we can say analytical understanding of thermal environment including both static and dynamic characteristics is inevitable to ensure the reliability of 3DS-ICs.

Acknowledgements

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References

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