PS-3-03

Switching Time Analysis of Negative Capacitance UTB GeOI MOSFETs

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Abstract

In this work, the impact of device parameters on the switching time and subthreshold swing of negative capacitance ultra-thin-body (UTB) Germanium-On-Insulator (NC-GeOI) MOSFETs is analyzed. NC-GeOI MOSFETs with smaller gate length (Lg), EOT, and buried oxide thickness(T_{box}) and thicker ferroelectric layer thickness (T_{FE}) exhibit larger subthreshold swing improvements over GeOI MOSFETs. Compared with GeOI MOSFETs, NC-GeOI MOSFETs exhibit better switching time due to improvements in effective drive current (I_{eff}) and subthreshold swing. NC-GeOI MOSFET exhibits larger ST improvements at Vdd = 0.3V (-82.9%) than at Vdd = 0.86V (-9.7%), because NC-GeOI MOSFET shows 18.2 times higher I_{eff} than the GeOI MOSFET at Vdd = 0.3V, while 2.5 times higher I_{eff} at Vdd = 0.86V. Therefore, NC-GeOI MOSFETs have more benefits when operating at low supply voltage for ultra-low power applications.

Introduction

The design of ultra-low power integrated circuits is important for portable electronics, implantable bio-medical devices, and energy harvesting system. Device with higher Ion/Ioff ratio is essential in order to achieve energy-efficient switching at given supply voltage. Negative capacitance FET (NCFET) [1] has been attracting interests because it reduces subthreshold swing below classical limit of ~60mV/dec, and therefore shows higher Ion/Ioff ratio. Negative capacitance ultra-thin-body MOSFETs (NC-UTB MOSFETs) have been analyzed for capacitance tuning and antiferroelectric operation [2-3]. The hysteresis-free design space for NC-UTB GeOI MOSFETs has been studied compared with Si counterparts [4]. However, switching time (ST) analysis of NC-GeOI MOSFET has rarely been discussed. In this work, the impact of device parameters (including Lg, EOT and T_{box}) and thickness of ferroelectric layer (T_{FE}) on the subthreshold swing (SS) and ST of the hysteresis-free NC-GeOI MOSFETs are analyzed and compared with the GeOI MOSFETs. Mobility and band-to-band tunneling model of UTB GeOI MOSFET are calibrated [6] in the TCAD simulations. Results show that compared with the GeOI MOSFETs at Vdd = 0.86V, the NC-GeOI MOSFETs exhibit significant improvements in SS while fewer improvements in ST due to the increased transition charge (ΔQ). However, as Vdd scales down to 0.3V, NC-GeOI MOSFETs show larger improvements in ST due to much higher I_{eff} improvements.

Subthreshold Swing of NC-GeOI MOSFETs

Fig. 1(a) illustrates the 2D NC-GeOI structure used in this work. Fig. 1(b) shows the Id-Vg characteristics of the baseline GeOI and NC-GeOI MOSFETs. The ferroelectric parameters of $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric layer, such as coercive electric field E_c = 1 MV/cm, remnant polarization P_0 = 17 μC/cm^2 [8] and T_{FE} = 8 nm, are used for NC-GeOI MOSFETs with hysteresis-free design. Fig. 2 shows the simulation flow of 2D TCAD coupled with 1D Landau-Khalatnikov (LK) ferroelectric equation for modeling the NC-GeOI MOSFETs [5]. Fig. 3 describes the simple capacitance model of NC-GeOI MOSFET and equations for analyzing the internal voltage amplification (Av), subthreshold swing (SS) and switching time (ST). According to the definition of internal voltage amplification (Av), capacitance underneath the ferroelectric layer (C_{mos}) should be closer to the capacitance of ferroelectric layer $|C_{FE}|$ in order to achieve higher Av and smaller SS of NC-GeOI MOSFETs. However, $|C_{FE}|$ cannot be smaller than C_{mos} to avoid hysteresis phenomenon. At external gate voltage of NC-GeOI MOSFET ($V_{g,ext}$) = 0 V, $|C_{FE}|$ can be described as $C_{FE} = dQ_g/dV_{FE} \approx 1/(2\alpha \cdot T_{FE})$.

The gate charge (Q_g) at $V_{g,ext}$ = 0 V is too small that the second term of V_{FE} shown in Fig. 2 can be ignored. The simplified equation of C_{FE} indicates that $|C_{FE}|$ is only related to ferroelectric parameters at low $V_{g,ext}$. Therefore, the C_{mos} is the key of capacitance matching for achieving better SS. Fig. 4 shows the impact of device parameters on the C_{mos}, $|C_{FE}|$ and SS for GeOI and NC-GeOI MOSFETs at Vds = 0.05 V. The inset of Fig. 4(a) shows that C_{mos} increases as Lg decreases from 100 nm to 20.2 nm. Therefore, the SS improvements of NC-GeOI MOSFETs over GeOI MOSFETs increase as Lg decreases. Compared with the GeOI MOSFETs, NC-GeOI MOSFETs show 32.7% (9%) SS improvements at Lg = 20.2 nm (Lg = 100nm). The SS improvement is defined as $[(SS_{NC\text{-}GeOI} - SS_{GeOI})/SS_{GeOI}]$. The inset of Fig. 4(b) shows that $|C_{FE}|$ decreases as T_{FE} increases. Therefore, the SS improvements increase with T_{FE}. With T_{FE} = 8nm, the NC-GeOI MOSFET shows 32.3% SS improvement. The inset of Fig. 4(c) shows that for NC-GeOI MOSFETs, reducing EOT increases C_{mos}, and therefore exhibits slightly larger SS improvement as EOT decreases. Decreasing T_{box} shows slightly larger C_{mos} and SS improvement as shown in Fig. 4(d).

Switching Time of NC-GeOI MOSFETs

In this section, the impact of device parameters on the switching time (ST) of NC-GeOI MOSFETs compared with GeOI MOSFETs is analyzed. The switching time is defined as ST = ΔQ /Ieff [7], where ΔQ is the transition charge between "on" and "off" states and given by the difference between Q_g (Vg = Vdd, Vd = 0.05V) and Q_g (Vg = 0, Vd = Vdd). I_{eff} is the effective drive current which is given by the average of I_d (Vg = Vdd, Vd = Vdd/2) and I_d (Vg = Vdd/2, Vd = Vdd). Fig. 5 (a) shows the impact of T_{FE} on the ST of NC-GeOI MOSFETs compared with GeOI MOSFETs. It can be seen that compared with GeOI MOSFET, NC-GeOI MOSFETs with thicker T_{FE} exhibit smaller ST and larger improvements in ST (17.7% at T_{FE} = 10nm). This is because as T_{FE} increases, the increase in I_{eff} is more significant than the increase in ΔQ for NC-GeOI MOSFETs as shown in Fig. 5(b). Reducing EOT improves the SS of NC-GeOI MOSFETs (Fig. 4(c)). However, Fig. 6(a) shows that reducing EOT slightly increases the ST of NC-GeOI MOSFETs. This is because as EOT decreases, the increase in ΔQ is slightly higher than the increase in I_{eff} for NC-GeOI MOSFETs as shown in Fig. 6(b). Besides, the ST of GeOI MOSFETs slightly increases with EOT because the reductions of I_{eff} is slightly larger than the reduction in ΔQ as EOT increases. In other words, NC-GeOI MOSFETs exhibit better ST as EOT increases, although SS decreases with EOT. Fig. 7(a) shows that the ST of GeOI and NC-GeOI MOSFETs increase as T_{box} decreases because the I_{eff} degrades intensely with reducing T_{box} (Fig. 7(b)). Compared to GeOI MOSFET with T_{box} = 2 nm, NC-GeOI MOSFET still shows smaller ST (59.3% improvement in ST) because of larger I_{eff}. Fig. 8(a) and 8(b) show the impact of Lg on the ST of GeOI and NC-GeOI MOSFETs at Vdd = 0.86V and Vdd = 0.3V, respectively. As Lg decreases, ST decreases due to decreasing ΔQ and increasing I_{eff}. Compared with GeOI MOSFETs at Vdd = 0.86V, NC-GeOI MOSFETs show 36.1% improvement in ST at Lg = 100 nm and 9.7% improvement in ST at Lg = 20.2 nm. Compared with GeOI MOSFET with Lg = 20.2 nm, NC-GeOI MOSFET exhibits significant ST improvement at Vdd = 0.3V (-82.9%) and slightly ST improvement at Vdd = 0.86V (-9.7%). This is because at Vdd = 0.3V and Lg = 20.2 nm, NC-GeOI MOSFET exhibits 18.2 times higher I_{eff} than the GeOI MOSFET; while at Vdd = 0.86V, NC-GeOI MOSFET shows 2.5 times larger I_{eff} than the GeOI MOSFET. In other words, NC-GeOI MOSFETs show more benefits when operating at low supply voltage.

Acknowledgments

This work is supported by the Ministry of Science and Technology in Taiwan under Contracts MOST 105-2628-E-008-006-MY3 and 105-2622-8-002-001.

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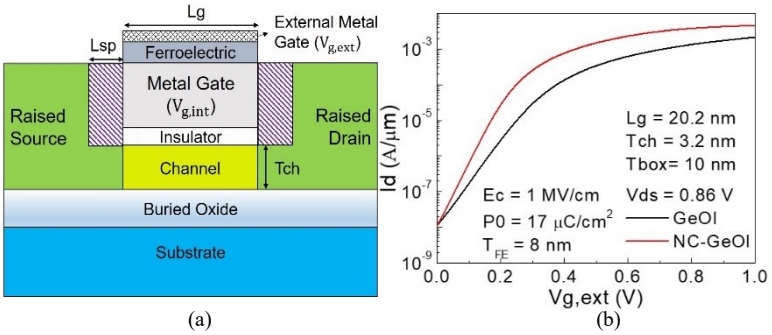

Fig. 1. (a) The 2D NC-GeOI structure used in this work. $V_{g,ext}$ is the voltage of external metal gate. $V_{g,int}$ is the voltage of internal metal gate. (b) The Id-Vg characteristics of the TCAD baseline UTB-GeOI and NC-GeOI MOSFETs. The NC-GeOI is modeled based on the baseline GeOI and LK equation. At Vds = 0.86 V, NC-GeOI and GeOI MOSFETs are designed to have the same I_{off} for a fair comparison. The ferroelectric parameters are extracted from $Hf_{0.5}Zr_{0.5}O_2$. [8]

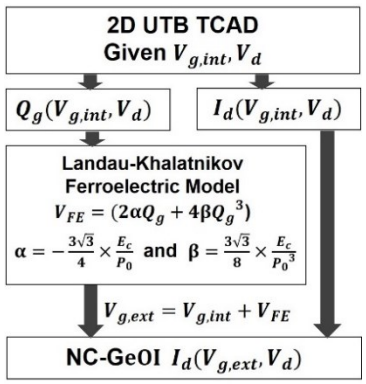

Fig. 2. 2D TCAD GeOI MOSFET simulation coupled with 1D-LK equation is used to model NC-GeOI MOSFET. [5]

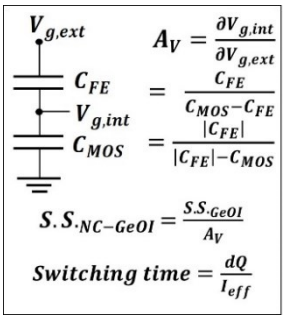

Fig. 3. The capacitance model of NC-GeOI MOSFET and the equations of voltage amplification factor (Av), subthreshold swing (S.S.) and switching time. I_{eff} is the effective current and dQ is the transition charge [7].

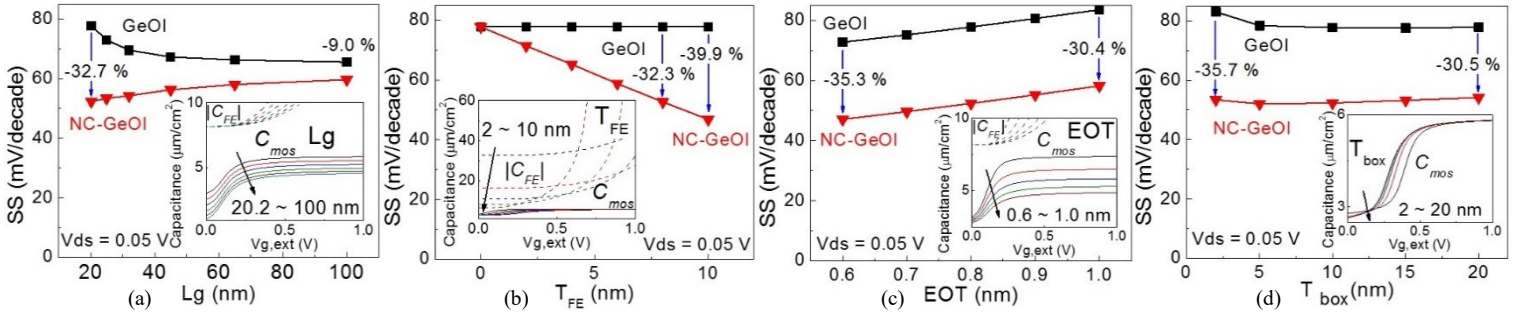

Fig. 4. Impacts of (a) Lg, (b) T_{FE}, (c) EOT and (d) T_{box} on the SS and the capacitances at Vds = 0.05V. C_{mos} is the capacitance of the device underneath the ferroelectric layer and $|C_{FE}|$ is the capacitance of ferroelectric layer. For NC-GeOI MOSFET at $V_{g,ext}$ = 0 V, C_{mos} should be close to its $|C_{FE}|$ to achieve higher Av and larger improvement in SS compared to the baseline GeOI MOSFET.

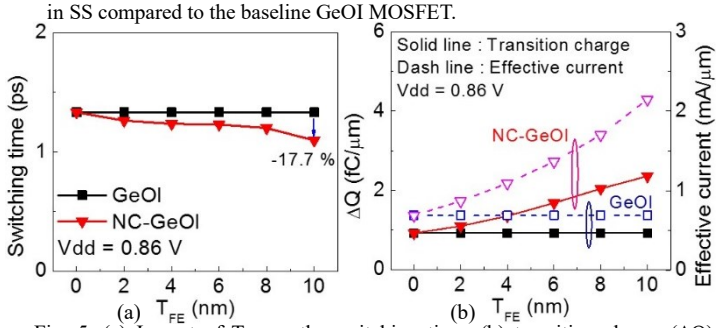

Fig. 5. (a) Impact of T_{FE} on the switching time, (b) transition charge (ΔQ) and effective current (I_{eff}). NC-GeOI MOSFETs with thicker T_{FE} show lower switching time than GeOI MOSFETs, because NC-GeOI MOSFETs show much larger I_{eff} in spite of larger ΔQ compared with the GeOI MOSFETs.

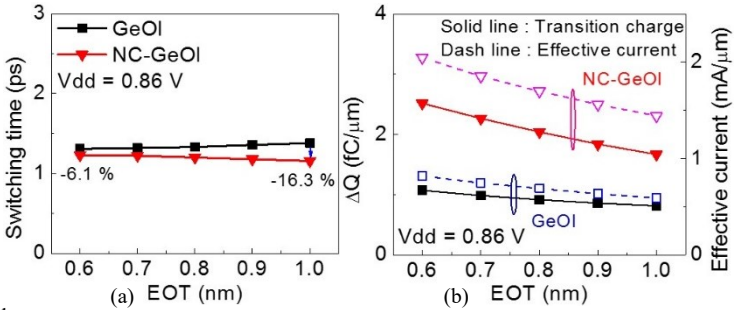

Fig. 6. (a) Impact of EOT on the switching time, (b) ΔQ and I_{eff}. As EOT scales, NC-GeOI MOSFETs show slightly increase in switching time because the increase in ΔQ is more than the increase in I_{eff} as EOT reduces.

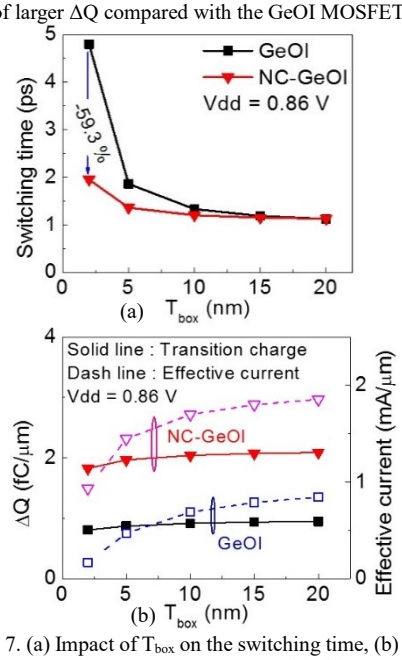

Fig. 7. (a) Impact of T_{box} on the switching time, (b) ΔQ and I_{eff}. GeOI and NC-GeOI MOSFETs with thinner T_{box} show larger switching time because of degraded I_{eff}. Compared to GeOI MOSFET with T_{box}=2 nm, NC-GeOI MOSFET still exhibits better switching time due to larger I_{eff}.

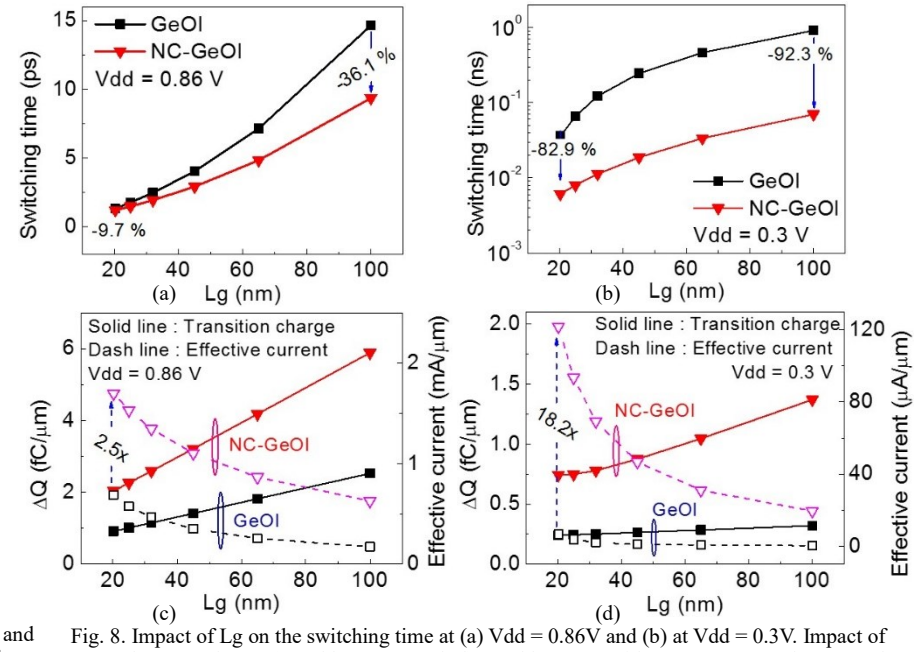

Fig. 8. Impact of Lg on the switching time at (a) Vdd = 0.86V and (b) at Vdd = 0.3V. Impact of Lg on the ΔQ and I_{eff} at (c) Vdd = 0.86V and (d) at Vdd = 0.3V. With Lg = 20.2nm and compared with GeOI MOSFET, NC-GeOI MOSFET shows 9.7% improvement in switching time at Vdd = 0.86V, and 82.9% improvement in switching time at Vdd = 0.3V. NC-GeOI MOSFET exhibits significant advantages in switching time at low Vdd compared with the GeOI MOSFET.