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Short Channel Modeling of Tunnel FET's

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Abstract

Short channel effects of tunnel FETs are investigated in detail using device simulation with the nonlocal band to band tunneling model. Discussions are based on silicon, and are divided into several simulation scenarios in order to distinguish different effects such as source overlap and drain offset. When the drain offset is adopted to suppress the drain leakage current, the short channel effects are suppressed. The physical understanding of the TFETs' short channel behaviors is clearly different from those of MOSFETs. Finally the minimum gate length to obtain on currents is proved to be 3nm for single gate and 2nm for double gate based on the drain offset structure.

1. Introduction

Tunnel FET (TFET) is widely studied for low power applications beyond CMOS. Although there are some articles concerning the short channel effects (SCE) of TFETs [1-4], the discussions are still insufficient. It is because that the channel of the TFET differs from that of the MOSFET but is a part of a PN-junction. The authors have already been simulated several cases of TFETs based on SOI technologies, and have verified the accuracy and validity of the non-local band to band tunneling (BTBT) model [5] implemented in the device simulator [6]. In the previous work, authors have discussed the drain bias dependencies of long channel TFETs [7]. In this work, SCE of TFETs are investigated in detail.

2. Simulation Method

The simulation assumed a typical simple SOI device structure based on silicon technologies as shown in Fig. 1, where source overlaps L_{OVS} and drain offsets L_{OFFD} are assumed. This is a p-type TFET, with the p-type channel same to drain type, and a *PN*-junction is located at the source side.

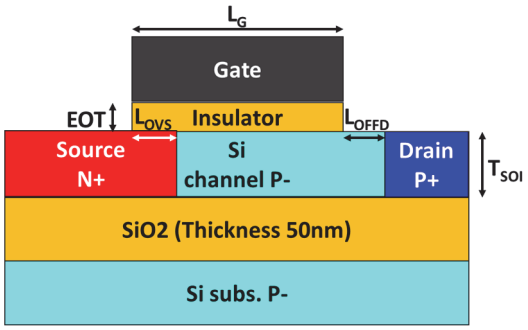

Fig. 1 An SOI device structure assumed in this work, with some important notations.

3. Simulation Results and Discussions

We focus on the supply voltage of 0.5 V for low power applications. To clarify SCE, the gate work function is optimized to match the long channel I_{OFF} to 10^{-13} A/μm. This leakage value may depend on the semiconductor material parameters. Since the definition of the threshold voltage may cause discussions, we evaluate SCE by I_{ON} and I_{OFF}.

It is another problem how to determine simulation scenarios to investigate TFET SCE. We have decided to consider several scenarios which are discussed independently.

The First Scenario – Overlapped Source and Drain

The first scenario is the case that both source and drain impurities are overlapped to the gate in order to understand the effects of source to drain distances.

1) Source and drain are abrupt, 2×10^{20}/cm^3, and overlapped to the gate.
2) Channel is p-type and 3×10^{14}/cm^3.
3) The source to drain distance is changed while the gate length is fixed to 70nm.

Fig. 2 shows I_{OFF} vs the source to drain distance (L_{SD}) for several T_{SOI} and EOTs. It is clarified that thinner T_{SOI} and slightly suppresses SCE, but EOT does not.

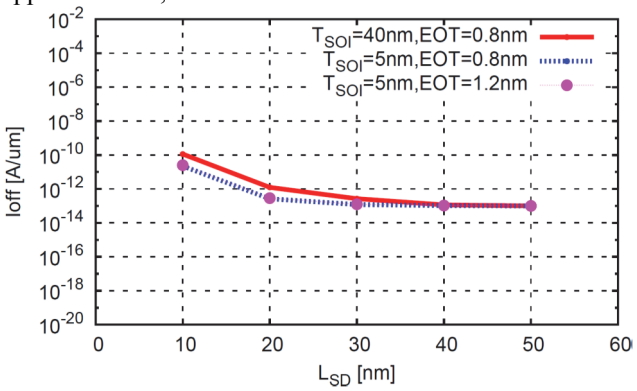

Fig. 2 I_{OFF} vs L_{SD} for several T_{SOI} and EOT conditions.

The Second Scenario –Drain Offset Dependence

In the second scenario, the effects of drain offset are investigated.

1) Source and drain are abrupt, 2×10^{20}/cm^3, and the source overlap is fixed to 10nm.
2) The gate length is fixed to 30nm.
3) The channel is p-type and 3×10^{14}/cm^3.
4) The drain offset is changed.

In Fig. 3, I_{OFF} vs L_{SD} for this scenario is compared to that of the first scenario. Both results are identical. In the same figure, the on current I_{ON} is also

plotted using the right linear axis. It is interesting that I_{ON} does not depend on the drain offset lengths and depend only on the source to drain distance L_{SD}. The reason is that TFET is a *PN*-diode.

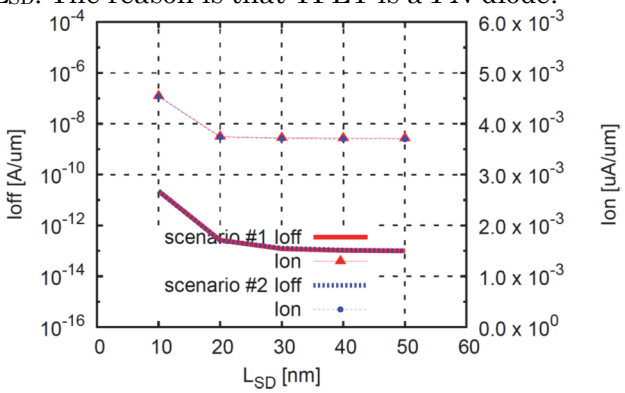

Fig. 3 I_{OFF} and I_{ON} vs L_{SD} of the second scenario are identical to the first scenario. T_{SOI} is 5nm and EOT is 0.8nm.

The Third Scenario – Fixed Offset Drain

The third scenario is the case of 30nm offset drain which is a typical design to reduce the off leakage current arising from drain side tunneling. This scenario is not common in the MOSFET design.

1) Source and drain are abrupt, 2×10^{20}/cm^3, source overlap L_{OVS} is 0nm and drain offset L_{OFFD} is 30nm.
2) T_{SOI} is 5nm and the channel is p-type 3×10^{14}/cm^3.
3) The gate length L_G is changed.

Fig. 4 shows I_{OFF} vs L_G of this scenario compared to the first scenario. In this scenario, the off leakage currents are not affected by the gate lengths. I_{ON} is also plotted using the right linear axis. While for the first scenario, both I_{OFF} and I_{ON} increase at 10nm L_{SD}, for the second scenario, I_{OFF} and I_{ON} weakly changed at 10nm L_G. Although there is no gate length merit of the on currents of TFETs, the gate length should be scaled to suppress gate capacitances and device areas.

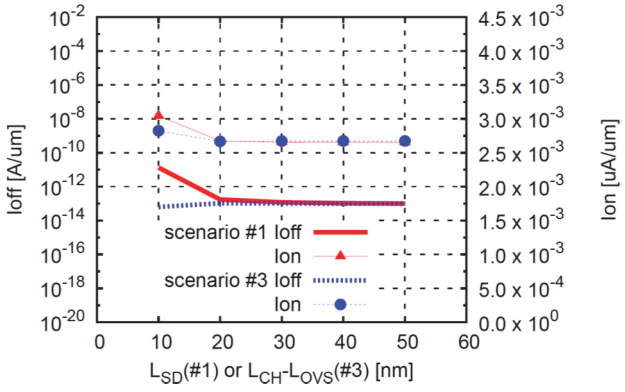

Fig. 4 I_{OFF} vs L_G of the third scenario compared to I_{OFF} vs L_{SD} of the first scenario. T_{SOI} is 5nm and EOT is 0.8nm.

Fig. 5 shows the comparison of the single gate SOI TFET to the double gate TFET, simulated by the third scenario. When I_{OFF} is configured to the same value, there is more than double I_{ON} merit in the double gate case, because of the stronger gate control of the tunnel band bending.

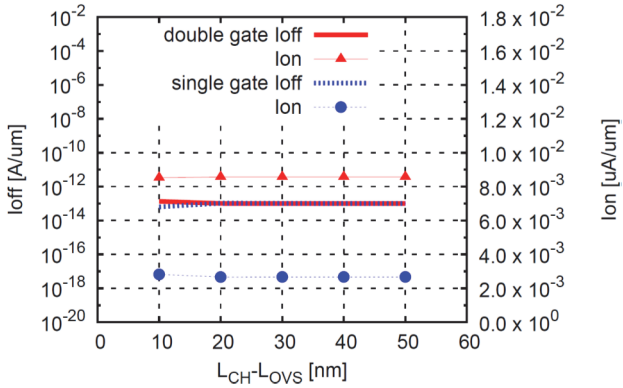

Fig. 5 I_{OFF} vs L_G of the third scenario for single and double gate.

The Fourth Scenario – Minimum Gate Length

The fourth scenario is to clarify the minimum gate length based on 0nm source overlap and 30nm drain offset. Fig. 6 shows the I_{ON} vs the gate length of this scenario. Keeping the long channel I_{OFF}, the I_{ON} decreases from 8nm for single gate and 6nm for double gate. The minimum gate lengths to obtain I_{ON} is 3nm for the single gate and 2nm for the double gate.

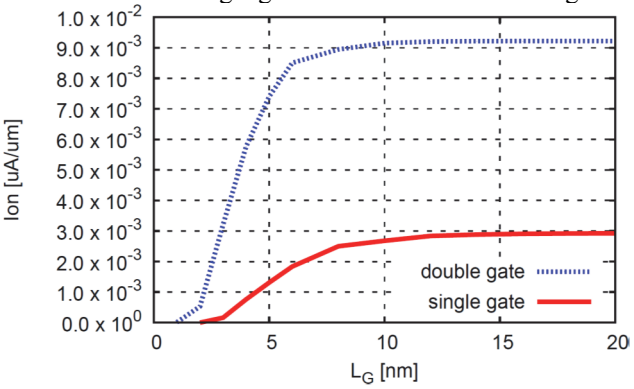

Fig. 6 I_{ON} vs L_G of the fourth scenario for single and double gate.

3. Conclusions

Short channel effects of silicon SOI tunnel FETs are discussed for the supply voltage of 0.5 V using device simulations. The gate work function is optimized to match the long channel I_{OFF} to 10^{-13} A/um, and the short channel effects are discussed on the short channel I_{OFF}'s and I_{ON}'s. While I_{OFF} depends on the source to drain distance below 10nm, the gate scaling merit of I_{ON} is not observed. To obtain the gate capacitance merit, the gate length should be minimized with 30nm drain offset. The double gate I_{ON} is more than double of the single gate. Finally the minimum gate length is 3nm for single gate and 2nm for double gate.

Acknowledgements

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References

[1] L. Liu, et al., DRC, 2010. [2] J. Wu, et al., TED, 2015.
[3] N. D. Chien, et al., Microelectronics Reliability, 2015.
[4] W. Lin, et al., JJAP, 2016. [5] K. Fukuda, et al., SISPAD, 2012.
[6] HyENEXSS [7] K. Fukuda, et al., SSDM, 2016.