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Improved Hetero-Gate-Dielectric Tunnel Field-Effect Transistors

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Abstract

The design of hetero-gate-dielectric tunnel field-effect transistors (HG TFETs) is improved from our previous work by using two key fabrication steps: HF vapor etch and sidewall spacer formation. The improved electrical characteristics are confirmed by both simulation and experimental results.

1. Introduction

Recently, a tunnel field-effect transistor (TFET) has been considered one of the most promising solutions to extremely-low-power applications. TFETs show low off-current (I_{off}) and sub-60mV/dec *SS* at room temperature because their operation is based on band-to-band tunneling. On the other hand, TFETs have disadvantages such as low on-current (I_{on}) and ambipolar behavior [1, 2]. Previously, we proposed and implemented hetero-gate-dielectric (HG) TFETs which show higher I_{on} and smaller *SS* than conventional TFETs by simply replacing source-side gate insulator with high-k materials [3, 4]. However, previous prototype HG TFETs showed lower performance than predicted due to the following three reasons: enlarged high-k dielectric thickness at the source side, sidewall spacer structure and gradual source doping profile [5]. In this manuscript, the design of HG TFETs is improved and their characteristics are evaluated by using simulation and experimental data. To realize the structure, two improved fabrication methods were adopted: HF vapor etch and HfO_2 dry etch processes.

2. Proposed Solutions

Previous prototype HG TFETs could not show the expected performance due to two structural issues. First, sidewall spacer structure is problematic. Because of HfO2 remained under the sidewall spacer, source region potential is controlled by the gate bias due to fringing field. Thus, electric field of tunneling junction is lowered and finally onset voltage (V_{onset}) and *SS* have larger values. Second, previous SiO_2 etch technique with 7:1 BHF solution is problematic. Source-side corner of the gate is etched during gate insulator etch process. Thus, the thickness of HfO_2 was larger than the thermally grown gate oxide thickness (T_{ox}) and the gate-to-channel coupling strength is reduced.

In order to evaluate performance improvement, 2D simulations were performed with SILVACO ATLAS. Figs. 1a and 1b indicate the prototype and improved HG TFET structures, respectively. To demonstrate the structural enhancement, we compared them when turned-on, both gate voltage (V_G) and drain voltage (V_D) are equal to 0.7 V. Figs. 1c and 1d show the electric field contour of improved and prototype HG TFET. Improved HG TFET is more robust to fringing field effects and electric field is highly concentrated near the junction.

For the fabrication of the improved version of HG TFETs, two fabrication methods were adopted. First, HF vapor etch process is introduced. Through the vapor phase etch technique, thickness uniformity between SiO_2 and HfO_2 is bettered because HF vapor has much higher selectivity of SiO_2 to silicon and poly-silicon wet etch process with 7:1 BHF solution. Second, HfO2 etch step is added to suppress the fringing field over the tunneling junction. This step is added between HfO_2 atomic layer deposition (ALD) and sidewall spacer forming. To protect the HfO_2 layer inserted under the gate, anisotropic HfO_2 etch process was defined. Fig. 2 shows the key process flow to form HG and spacer structure of prototype and improved HG TFETs.

Fig. 3a and b show the cross-sectional transmission electron microscope (TEM) images of the fabricated HG TFET. $L_{high\text{-}k}$ of the fabricated HG TFET is ~7 nm which is similar to the optimized value [13]. Additionally, the increase of $THfO_2$ at the source was improved and HfO_2 layer on the source was removed in the improved HG TFETs as shown in Fig. 3a. THfO2 is almost equal to $TSiO_2$. The spacers consist of 3-nm-wide inner HfO_2 spacers and 20-nm-wide outer TEOS spacers. In order to evaluate the merits of HG TFETs, SiO_2-only TFETs were also fabricated as control devices. Most of the process flow was the same as that of HG TFETs except for the formation of the HG structure. The SiO_2-only TFET has only 20-nm TEOS spacers.

3. Results and Discussion

Fig. 4a illustrates the transfer curves of the improved HG TFETs compared with those of prototype HG TFETs and SiO_2-only TFETs. Improved HG TFETs show higher I_{on} and lower *SS* than prototype HG TFETs as a result of device design improvement. It is because gate dielectric thickness is remained same as T_{ox} at source-side end and high-k material is removed over source region. This reduces tunneling width and concentrate the electric field at the tunneling junction. Fig. 4b shows *SS* of improved and prototype HG TFETs in terms of drain current (I_D). SS of SiO_2-only TFETs is not considered because SS is much higher than those of both HG TFETs. Improved HG TFETs show lower SS in all drain current level compared to prototype HG TFETs. Table 1 summarizes extracted electrical parameters of improved HG TFET compared to those of prototype HG TFET and SiO_2-only TFET.

4. Summary

In this work, HG TFETs' structure have been optimized through the simulation and fabrication in order to demonstrate its possibility of higher performance and low-power consumption. As a result, improved HG TFETs shows ~12x higher I_{on}, ~0.77x lower *SS* and suppressed Iamb than our prototype work. In conclusion, HG TFETs are promising to be used for highly energy efficient ICs.

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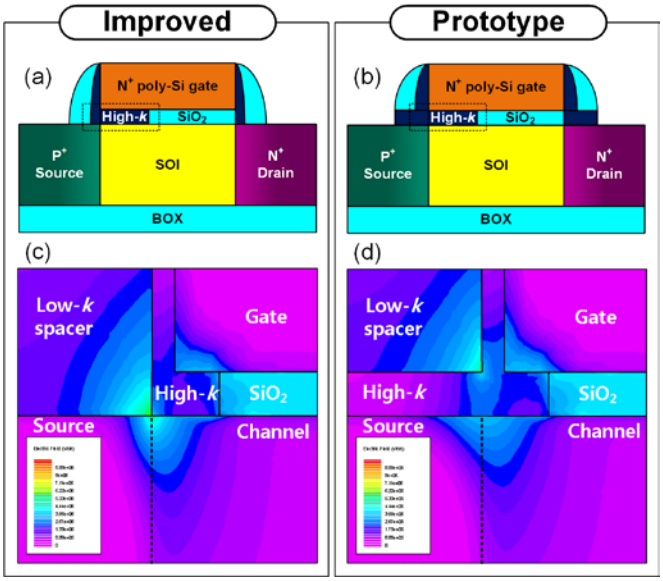

Fig. 1. Comparison of prototype and improved HG TFET. Improved HG TFETs' (a) Device structure. (b) Electric field contour near source-channel junction. And prototype HG TFETs' (c) Device structure. (d) Electric field contour near source-channel junction. The improved HG TFET is more robust to fringing field effect and electric field is concentrated near the junction.

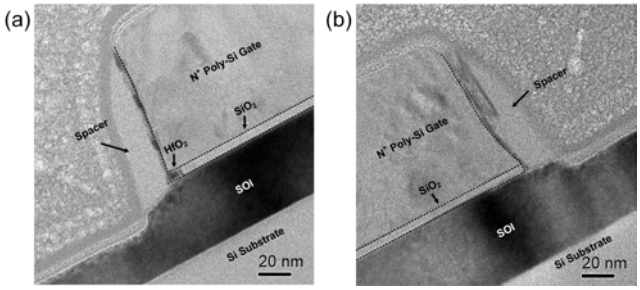

Fig. 3. Cross-sectional TEM image of the fabricated HG TFET in (a) source-side and (b) drain-side.

Table 1. Electrical characteristics of improved, prototype HG TFET, and SiO_2-only TFET.

	Improved HG TFET	Prototype HG TFET	SiO_2-only TFET
L_G, W_G (μm)	1.0, 2.7	1.0, 2.7	1.0, 2.7
T_{ox} (nm)	5	3	5
V_{DD} (V)	1	1	1
I_{on} (nA/μm)	56	18	0.004
I_{min} (pA/μm)	0.03	0.1	0.001
SS_{min} (mV/dec)	171	186	550
SS_{avg} (mV/dec)	176	215	650
I_{on}/I_{off}	$5.6x10^4$	$1.8x10^4$	3.5x10

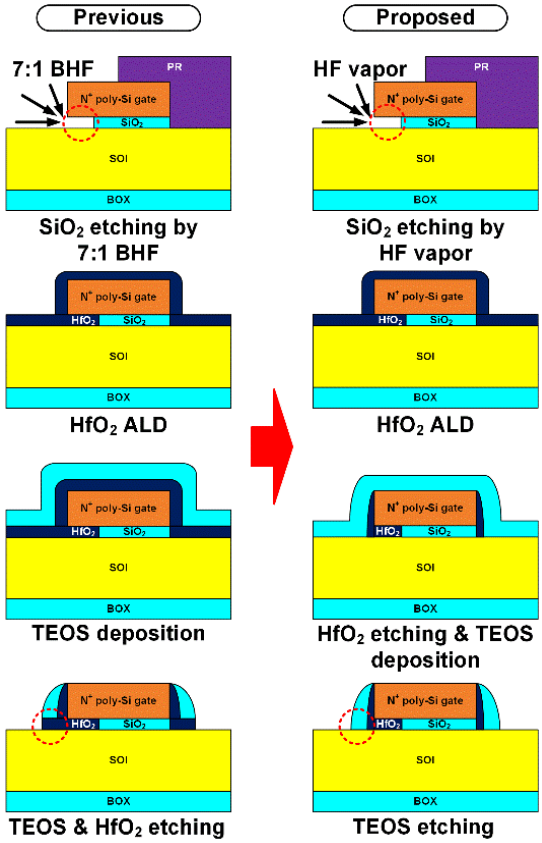

Fig. 2. Key processes modification for fabricating improved HG TFETs.

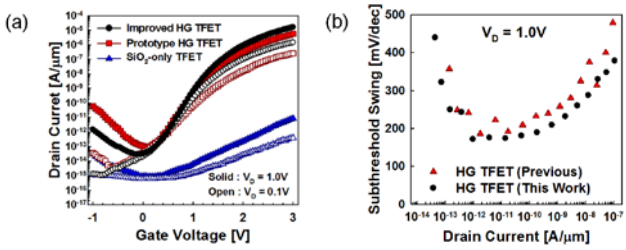

Fig. 4. (a) Transfer characteristics of the improved and prototype HG TFETs and SiO_2-only TFETs. (b) *SS* of the improved and prototype HG TFETs in terms of I_D.