Effects of Si Recess Structure on Performance and Reliability in High Voltage n-MOSFETs

Chun-Yen Chen1, Jone F. Chen1, Yen-Lin Tsai1, Hao-Tang Hsu2 and Hann-Ping Hwang2

1Institute of Microelectronics, Department of Electrical Engineering, National Cheng Kung University, Tainan 701, Taiwan
Phone: +886-6-2757575 ext.62400-1223 E-mail: yanlintsai@gmail.com
2Powerchip Technology Corporation, Hsinchu Science Park, Hsinchu 300, Taiwan

Abstract
Device characteristics and hot-carrier reliability of high voltage n-MOSFETs with various Si recess depths introduced by sidewall spacer over-etch are investigated. Experimental results show that the depth of Si recess has small effect on device characteristics. A device with a deeper Si recess has a smaller substrate current but produces a greater hot-carrier degradation. TCAD simulation results suggest that this unexpected result is caused by the severity in plasma damage during sidewall spacer over-etch and the difference in topology.

1. Introduction
It has been reported that plasma-induced Si recess structure has impact on the threshold voltage (Vt) of advanced nMOSFETs [1]. Previous studies discussed this issue by theoretical analyses and TCAD simulations. In this paper, the effects of Si recess structure introduced during sidewall spacer etching process on device characteristics and hot-carrier reliability of high-voltage n-MOSFETs are discussed. Both experimental data and TCAD simulation results are presented and analyzed.

2. Experimental Methods
The schematic cross section of the high-voltage n-type MOSFETs used in this study is shown in Fig. 1. To achieve the required off-state breakdown voltage, the lengths of poly-gate and N drift region (Ld) are roughly 0.9 µm and 0.7 µm, respectively. The gate oxide thickness is about 40 nm. Fig. 2 shows the schematic process flow that leads to Si recess structure in this paper. When defining the spacer region after N-drift implantation and TEOS deposition, Si recess structure is introduced during sidewall spacer etching. The depth of Si recess is mainly affected by the time of over-etch. In this paper, three different depths in Si recess (roughly 5~20 nm) are fabricated and denoted by device A, B, and C. Device A has the shallowest recess depth and device C has the deepest recess depth. Device characteristics including, linear-region drain current (Idlin), saturation-region drain current (Idsat), maximum transconductance (Gmmax), and Vt are measured. Idlin is measured at drain voltage (VD) of 0.1 V and gate voltage (VG) of 3.3 V. Idsat is measured at VD = 0.1 V. The hot-carrier stress is applied under VD = 10 V at VG that produces the peak substrate current (Isub). Stress tests are interrupted periodically to measure the degradation of the device.

3. Results and Discussions
The effects of Si recess on device characteristics are shown in Fig. 3, where Id-VG characteristics of devices A, B, and C measured at VD = 0.1 V are shown. The difference in Id-VG curves is small, indicating that Idlin, Gmmax, and Vt are almost the same. Id-VG measured at VD = 3.3 V (data not shown) also shows small difference in Idsat. Results mentioned above reveal that the depth of Si recess has small effect on device characteristics in our devices.

To examine hot-carrier reliability of the device, Isub-VG characteristics of devices are measured at VD = 10 V and shown in Fig. 4. The peak Isub occurs at VG around 2.9 V. It is clear that a deeper Si recess (recess A < B < C) results in a smaller Isub. Isub-VG measured at VD = 10 V and VG = 2.9 V (peak Isub condition) for 1000 seconds. Idlin degrades the most, suggesting that hot-carrier induced damage is mainly located in the N region [2].

Fig. 1 Schematic cross section of the device used in this paper.
Fig. 2 Schematic process flow that leads to Si recess structure.
Fig. 3 Id-VG curves of devices with various depths in Si recess.

Fig. 4 Isub-VG curves of devices with various depths in Si recess.
The effect of Si recess depth on hot-carrier induced degradation is shown in Fig. 6, where $I_{\text{Dlin}}$ degradation of devices stressed under $V_D = 10 \text{ V}$ and $V_G = 2.9 \text{ V}$ is compared. A deeper Si recess results in a larger $I_{\text{Dlin}}$ degradation. The inset of Fig. 6 shows the device lifetime vs. $1/V_D$, where lifetime is the time to reach 10% $I_{\text{Dlin}}$ degradation. It is also clear that a deeper Si recess results in a shorter lifetime. Since $I_{\text{sub}}$ value is usually used to judge the severity of device degradation [3], results shown in Fig. 6 is unexpected. In other words, device C has the largest $I_{\text{Dlin}}$ degradation even though its $I_{\text{sub}}$ is the smallest as in Fig. 4.

To investigate such an unexpected result, calibrated TCAD simulations are performed. Fig. 7 shows the impact ionization (I-I) rate of devices A and C biased at $V_D = 10 \text{ V}$ and $V_G = 2.9 \text{ V}$ (the stress condition in Fig. 6). The I-I rate of device A is larger than device C, which is consistent with $I_{\text{sub}}$ data in Fig. 4. Besides, the maximum I-I rate occurs under the spacer, i.e. in the N’ drift region, which supports our previous argument that hot-carrier induced damage is mainly located in the N’ region. To evaluate the impact of hot-carrier induced damage on $I_{\text{Dlin}}$ degradation, Fig. 8 shows the simulation results of $I_{\text{Dlin}}$ degradation vs. hot-carrier induced interface state ($N_i$), where acceptor-type $N_i$ is assigned near the Si-SiO$_2$ interface at the location where maximum I-I rate occurs (as in Fig. 7). From the stress result of device A at $t = 1000 \text{ s}$ in Fig. 6 (9.0% $I_{\text{Dlin}}$ degradation), it can be estimated from Fig. 8 that hot-carrier induced $N_i$ during stress is $9.6 \times 10^{11} \text{ cm}^{-2}$. For device C at $t = 1000 \text{ s}$ in Fig. 6 (10.3% $I_{\text{Dlin}}$ degradation), Fig. 8 reveals that $N_i$ produced in device C is $9.5 \times 10^{11} \text{ cm}^{-2}$. Such a result leads to the following two inferences. Firstly, during stress device C produces almost the same $N_i$ as in device A but device C has much smaller $I_{\text{sub}}$ as in Fig. 4. This may cause by the fact that traps are easier to create (near left-side of Si recess area denoted by D in Fig. 2) in device C due to more direct plasma interaction [4] during sidewall over-etch. Secondly, for the same amount of $N_i$, device C produces a larger $I_{\text{Dlin}}$ degradation. This may cause by the topology difference such that the impact of $N_i$ on $I_{\text{Dlin}}$ degradation is enhanced in a device with a deeper Si recess. From the above analyses, it is inferred that the larger hot-carrier degradation in a device with a deeper Si recess is caused by more plasma damage and the topology difference.

4. Conclusions

The device characteristics and hot-carrier reliability of high voltage n-MOSFETs with various Si recess depths introduced by sidewall spacer over-etch are presented. Results show that the depth of Si recess has small effect on device characteristics. A device with a deeper Si recess has a smaller $I_{\text{sub}}$ but produces a greater hot-carrier degradation unexpectedly. Our analyses suggest that the severity of plasma damage during sidewall spacer over-etch and the topology difference lead to this unexpected result.

References