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# Theoretical Investigation of the Performance Improvement in GeSn/SiGeSn hetero Line Tunneling FET (HL-TFET)

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**Abstract**

We demonstrate the performance improvement in GeSn/SiGeSn hetero line- tunneling field-effect transistor (HL-TFET) with the lattice-matched SiGeSn in the pocket region via numerical simulation. The HL-TFET achieves the smaller onset voltage ($V_{ONSET}$), the higher on-state current ($I_{ON}$) and the steeper subthreshold swing (SS) as compared with the GeSn homo Line TFET (L-TFET) and the conventional GeSn/SiGeSn double-gate hetero-TFET devices (H-TFET). The performance enhancement is mainly owing to the larger tunneling area in HL-TFET attributing to the presence of heterojunction and the tunneling junction (TJ) that perpendicular to the channel direction.

## 1. Introduction

Tunneling FET (TFET) which employs the band-to-band tunneling (BTBT) mechanism has been considered as one of the promising device candidates for ultralow power consumption applications [1]-[4]. However, the TFET still suffers from the insufficient on-state current ($I_{ON}$). GeSn has attracted tremendous research interests due to its ability that can transit from indirect to direct material by adjusting the Sn composition and the easy integration on Si platform [5]-[6]. High performance GeSn based TFET has been reported [7]-[9]. However, the performance of GeSn based TFET can be further improved by employing the structure optimization and the heterojunction engineering.

In this work, GeSn/SiGeSn hetero line-TFET (HL-TFET) is designed and characterized by simulation. As the lattice-matched SiGeSn used as the pocket material, the $I_{ON}$ and SS improvement of GeSn/SiGeSn HL-TFET is demonstrated owing to the larger tunneling area as compared with the GeSn homo line-TFET (L-TFET) and the conventional GeSn/SiGeSn double-gate hetero-TFET devices (H-TFET).

## 2. Device Design and Simulation Methodology

The schematic of GeSn/SiGeSn hetero line-TFET is shown in Fig. 1(a). Lattice-matched $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ was used to form the type-II staggered tunneling junction (TJ) with the conduction and valence band offsets of 29.8 and 162.5 meV, respectively [8]. The GeSn homo line-TFET and the conventional double-gate GeSn/SiGeSn hetero-TFET [Fig. 1(b)] were also simulated as the control devices. Self-consistent device simulations were carried out utilizing TCAD simulator, which implements a dynamic nonlocal tunneling algorithm. BTBT was calculated based on Kane's model [10]. Quantum confinement model provided by software was taken into account.

## 3. Electrical Results and Discussion

The Simulated $I_{DS}$-$V_{GS}$ curves of lattice-matched $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ hetero line-TFET (HL-TFET), $Ge_{0.92}Sn_{0.08}$ homo line-TFET (L-TFET) and conventional $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ hetero-TFET (H-TEFT) devices are shown in Fig. 2(a). The HL-TFET demonstrates sharper turn-on characteristic, and the enhanced drive current over its corresponding homo- and hetero- control transistors. Fig. 2 (b) shows the output characteristics for the TFET devices at $V_{GS}$ - $V_{TH}$ of 0.3 V. Here, $V_{TH}$ is defined as $V_{GS}$ at $I_{DS}$ of $10^{-11}$ A/μm. A 7 times higher $I_{ON}$, 24.9μA/μm, is achieved in GeSn/SiGeSn HL-TFET at $V_{DS}$ of 0.3 V, as compared with the H-TEFT, 3.1μA/μm. And, a 1.94 times higher $I_{ON}$ is obtained for HL-TFET in comparison with the GeSn homo line-TFET, 11.8μA/μm.

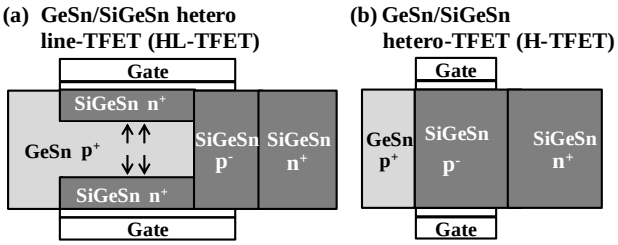


Fig. 1. Schematics of GeSn/SiGeSn hetero-line-TFET (HL-TFET) and the conventional GeSn/SiGeSn hetero-TFET (H-TFET) [8]. SiGeSn is embedded in the two pockets region to enlarge the tunneling current for the HL-TFET.

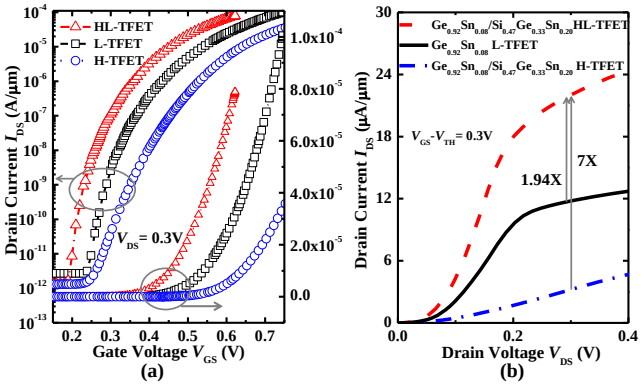


Fig. 2. Simulated (a) $I_{DS}$-$V_{GS}$ and (b) $I_{DS}$-$V_{DS}$ curves for $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ HL-TFET, H-TFET and the $Ge_{0.92}Sn_{0.08}$ homo line-TFET (L-TFET). The smaller $V_{ONSET}$, steeper SS and higher $I_{DS}$ can be observed for HL-TFET over the control devices.

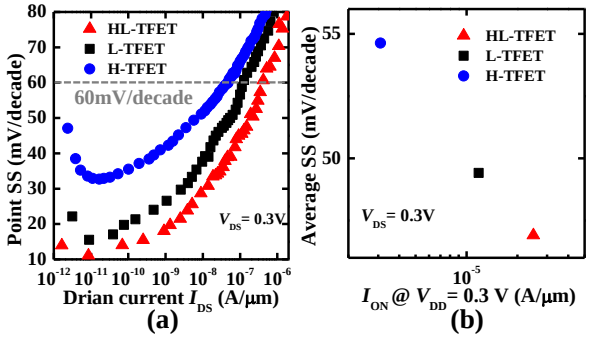


Fig. 3. (a) point SS as a function of $I_{DS}$ and (b) the average SS versus $I_{ON}$ at $V_{DS}$ of 0.3V for the HL-, L- and H-TFETs. The HL-TFET exhibits higher maximum $I_{DS}$ with sub-60mV/decade SS and smaller average SS over the H- and L-TFETs.

The improvement in point and average SS is achieved in HL-TFET as compared with the control devices [Figs. 3(a) and (b)]. Point SS obtained at each $V_{GS}$ is defined as $dV_{GS}/d(\lg I_{DS})$. The higher maximum $I_{DS}$ with sub-60 mV/decade SS is achieved in hetero line-TFET over homo- and the conventional hetero devices [Fig. 3(a)]. Average SS is extracted from $I_{DS}$-$V_{GS}$ curves, where $V_{GS}$ various from $V_{TH}$ to the value of $V_{TH}$+0.3 V. In comparison with the control devices, the HL-TFET exhibits the superior average SS characteristic owing to the larger tunneling current attributing to the larger tunneling area.

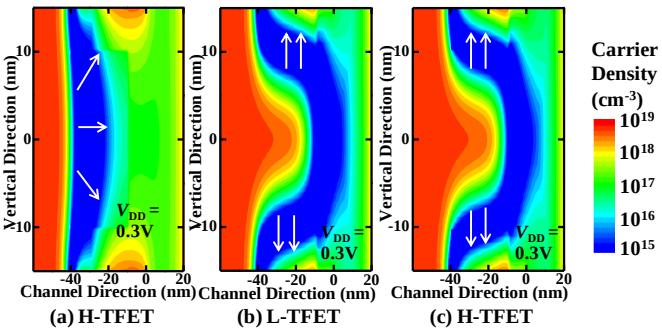


Fig. 4. Contour plots of carrier density for (a) $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ HL-TFET, (b) $Ge_{0.92}Sn_{0.08}$ L-TFET and (c) $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ H-TFET at $V_{DS}$=$V_{GS}$-$V_{TH}$=0.3V.

To illustrate the boosting effect of the device structure proposed in this work, the distribution of carrier density profiles for the devices at $V_{DD}$ = 0.3V are plotted in Fig. 4. The white arrow indicates the tunneling direction. It can be observed that, compared with the conventional hetero-TFET, the line-TFETs have no obvious advantage on the magnitude of the carrier density. But, it should be noted that, for the line-TFETs, the distribution areas of the maximum carrier density near the tunneling junction are almost located in the pocket region which contributes to the larger tunneling probability due to the fact that TJ is perpendicular to the channel direction in line-TFET as compared with the H-TFET.

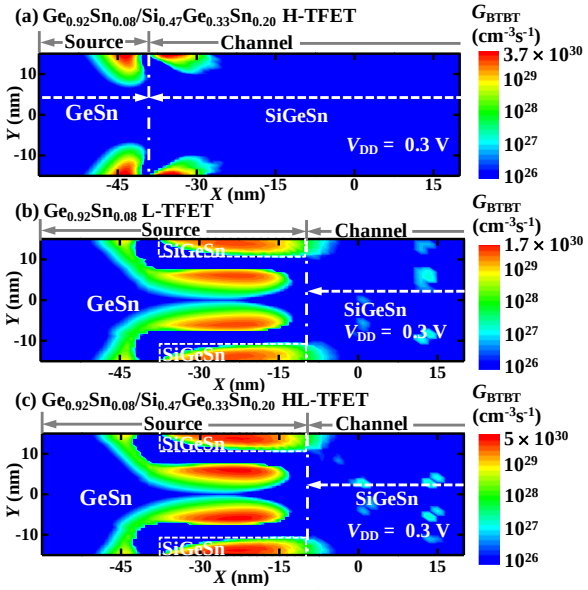


Fig. 5. Spatial distributions of $G_{BTBT}$ for (a) $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ HL-TFET, (b) $Ge_{0.92}Sn_{0.08}$ L-TFET and (c) $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ H-TFET at $V_{DS}$=$V_{GS}$-$V_{TH}$=0.3V. The HL- and L-TFET demonstrate larger peak $G_{BTBT}$ area over the H-TFET.

The impact of hetero-junction on BTBT of devices in on state is further analyzed by plotting the distribution of carrier generation rate $G_{BTBT}$ (Fig. 5), which directly determines the magnitude of tunneling current. At $V_{DD}$=0.3V, $Ge_{0.92}Sn_{0.08}$ homo line-TFET [Fig. 5(b)] demonstrates a slightly lower peak value of $G_{BTBT}$ compared to the $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ H-TFET [Fig. 5(a)]. While, it is also noticed that the maximum $G_{BTBT}$ centers in homo line-TFET have a larger distribution area than that in H-TFET owing to the fact that the tunneling junction is perpendicular to the channel direction due to the presence of the pocket region. Hence, the larger tunneling current is obtained in L-TFET in comparison

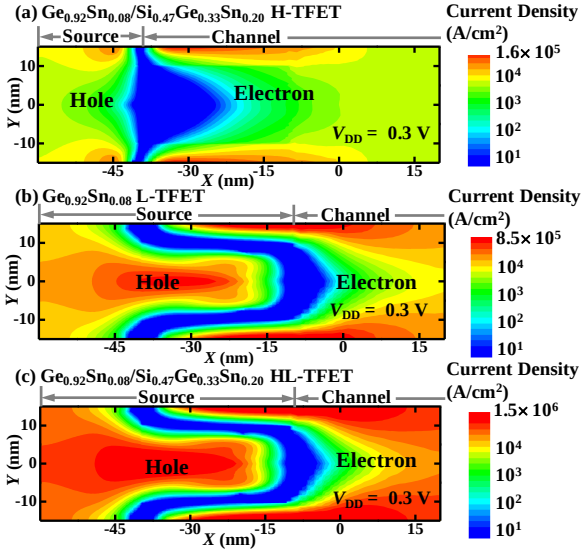


Fig. 6. Counter plots of the current density for (a) $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ HL-TFET, (b) $Ge_{0.92}Sn_{0.08}$ L-TFET and (c) $Ge_{0.92}Sn_{0.08}/Si_{0.47}Ge_{0.33}Sn_{0.20}$ H-TFET at $V_{DS}$=$V_{GS}$-$V_{TH}$=0.3V. The HL- and L-TFET obtain larger current density as compared with the H-TFET.

with the H-TFET. We can also observed that, the HL-TFET achieves even larger peak value of $G_{BTBT}$ due to the SiGeSn located in the pocket region contributing to the larger tunneling area and the shorten tunneling path [Figs. 5(b) and (c)].

In order to see the boosting effect of the heterojunction in HL-TFET directly, the distribution of current density for the devices are also plotted in Fig. 6. It can be observed that a higher peak value and a larger distribution area of the maximum current density centers is obtained in the line-TFETs than the H-TFET which is mainly owing to the TJ that perpendicular to channel direction leading to larger tunneling area. The hetero line-TFET demonstrates even larger peak value and distribution area of the maximum current density centers than the homo line device attributing to the presence of the SiGeSn located in pocket region leading to the shortened tunneling path and larger tunneling area which contributes to larger tunneling current.

## 4. Conclusions

GeSn/SiGeSn hetero line-TFET is designed and investigated. It is demonstrated that GeSn line-TFET achieves higher tunneling current than the H-TFET owing to the fact that the tunneling junction is perpendicular to channel direction leading to larger tunneling area. The GeSn/SiGeSn hetero line-TFET exhibits superior electrical characteristics than the homo line device attributing to the shortened tunneling path and the enlarged tunneling area induced by the SiGeSn located in the pocket region.

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