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Ge-cap Quantum Well Bulk FinFET for 5nm node CMOS Integration

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Abstract

We propose Ge-cap Quantum Well (QW) Bulk FinFET for 5nm CMOS integration, which is Si channel wrapped by Ge around three sides of the fin channel. The simulation results show that Ge-cap FinFET demonstrate better performance compare to pure Si, pure Ge, and Si-cap FinFET. By optimization of Si fin-width and Ge-cap thickness, the on-state current of nFET and pFET can also be symmetric without changing the total fin-width (F_{Wp}=F_{Wn}). The electrons density of Ge-cap concentrate in the Si channel because of QW formed in the conduction band of Si, while the holes density of Ge-cap pFinFET prefer to stay in Ge surfaces due to QW formed in the Ge valence band. The device physics studies of this device has enabled the design rules relevant for the application of CMOS inverter and SRAM application technology.

1. Introduction: As the transistor scaling down to 10nm technology node, the silicon-based FET had reached the fundamental physics and process technology limits. For increasing the device performance, high mobility channel materials have recently developed [1]. Germanium material is an alternative option to substitute Si because of high mobility, low temperature process; relative low cost, more symmetric with Si, and easier allows integration on Si platform [2]. For CMOS integration, the symmetrical drain saturation current is needed for NFET and PFET. Unfortunately, the electron mobility of Ge is approximately twice of hole mobility. In this paper, we propose the Ge-cap FinFET QW FinFET with the characteristic of on-state current is almost similar without changing the fin-width dimension for both NFET and PFET.

2. Device Structure and Simulation Models: Fig. 1.a and **1.b** presents the device structure of Ge-cap and Si-cap QW FinFET. The Ge-cap FinFET consists of Si as the channel material, which is wrapped by Ge around three sides of the fin channel. In contrast, the Si-cap FinFET uses Ge as the channel material, which is wrapped by Si. We compare the device performances of four devices structure: pure Si, pure Ge, Si-cap, and Ge-cap bulk FinFET (**Fig 1.c**). The parameters for the simulated device are tabulated in **Table 1**. The Sentaurus TCAD was used to perform 3D simulations, which included the density gradient (DG) model with quantum effects. Doping concentration-dependent SRH recombination, Matthiessen's rule mobility model, and BTBT model are considered. Fermi-Dirac distribution has been also activated.

3. Results and Discussion: Fig 2.a compares I_D-V_G characteristics of four devices structure at $|V_D|$=0.65 V and V_T=0.25V. Accordingly, the performance of Ge-cap FinFET is the best than the others device structure, both for NFET and PFET. The improvement of this structure is around 174% compare to pure-Si nFinFET. **Fig 2.a** shows that the characteristic of I_{ON} of Ge-cap is almost symmetric with the same fin-width (F_{Wp}=F_{Wn}=7nm) for both NFET and PFET. The normalized drain saturation current of Ge-cap is $1.8x10^{-4}$ A/µm and $1.7x10^{-4}$ A/µm for NFET and PFET, respectively. **Fig. 3** depicts that the electron/hole density of pure-Si and pure-Ge (NFET or PFET) under on-state condition is uniform in the whole channel region. On the other hand, the highest electron density of Si-cap NFET is located on the surface of the device. In contrast, the electrons in Ge-cap NFET concentrate in the Si channel because the electrons prefer to stay in the lower state of the conduction band (E_c) of Si channel. The electrons are trapped in the QW formed by E_c of Si and Ge (**Fig. 4b)**. The highest hole density of Ge-cap PFET is located in Ge surface channel material because the valence band (E_v) of Ge is lower than the Si (**Fig. 4.a)**. This structure can offer the advantages of high electron mobility of Si for NFET and hole mobility of Ge for PFET for CMOS integration. **Fig 5** shows that the voltage transfer characteristic (VTC) of Ge-cap is more symmetric between V_{IN} and V_{OUT} compare to the other structures. With different V_{DD}, the highest gain 38V/V can be achieved at V_{DD}=0.3V (**Fig 6)**. **Fig 7** presents butterfly curves and high static noise margin (SNM) values (146mV) of Ge-cap QW FinFET 6T SRAM cells during read access.

4. Conclusions: Ge-cap QW FinFET demonstrated better performance compare to pure Si, pure Ge, and Si-cap FinFET. By optimization Si fin-width and Ge thickness of Ge-cap FinFET, the characteristic of on-state current can be almost similar (balance). This proposed device structure can be alternative structure for future CMOS technology.

References: [1] H.Wu, et.al, IEDM (2014) 227. [2] S. Takagi et.al, Symp. on VLSI Tech. (2010) 147.

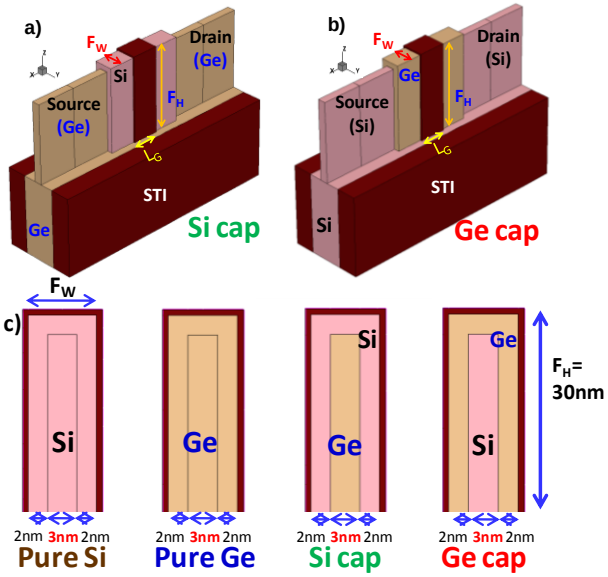

Fig. 1 Device structure of simulated a) Si-cap b) Ge-cap FinFET, and c) cross-section of pure Si, pure Ge, Si-cap, and Ge-cap FinFET

Table I. Device parameters used in the simulation

Parameters	Values [unit]
Channel length, L_G	10 [nm]
Fin height, F_H	30 [nm]
Total fin-width (both for NFET and pFET), F_W	7 [nm]
Effective Oxide Thickness, EOT	0.6 [nm]
S/D doping (As for NFET, B for PFET)	1×10^{20} [cm^{-3}]
Channel doping (B for NFET, As for PFET)	5×10^{17} [cm^{-3}]
Bulk doping (Boron, p-type)	5×10^{17} [cm^{-3}]

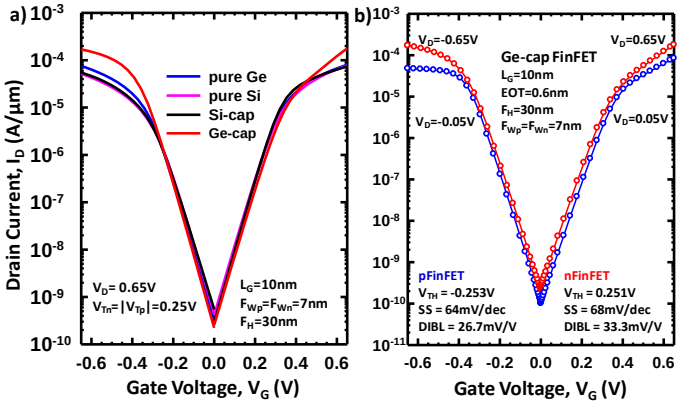

Fig. 2 a) Comparison of I_D-V_G curve of pure Si, pure Ge, Si-cap, and Ge-cap FinFET and b) transfer characteristics I_D-V_G curve of Ge-cap QW FinFET with L_G=10nm, F_H=30nm, and F_{Wn}=F_{Wp}=7nm

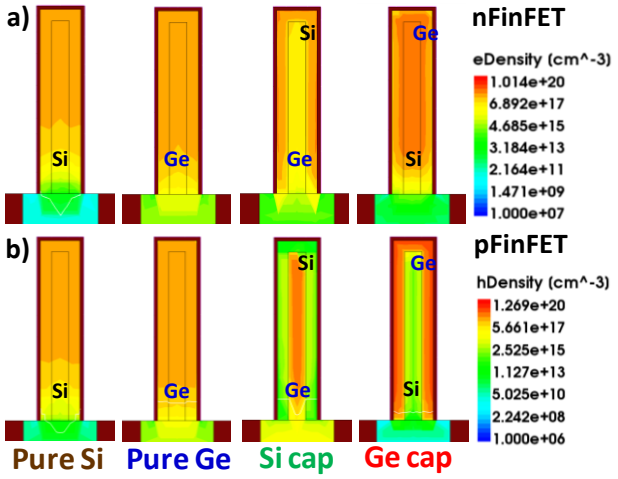

Fig. 3 a) Electron density of nFinFET and b) hole density of pFinFET for pure Si, pure Ge, Si-cap, and Ge-cap devices respectively under on-state condition ($|V_D|$=$|V_G|$=0.65V).

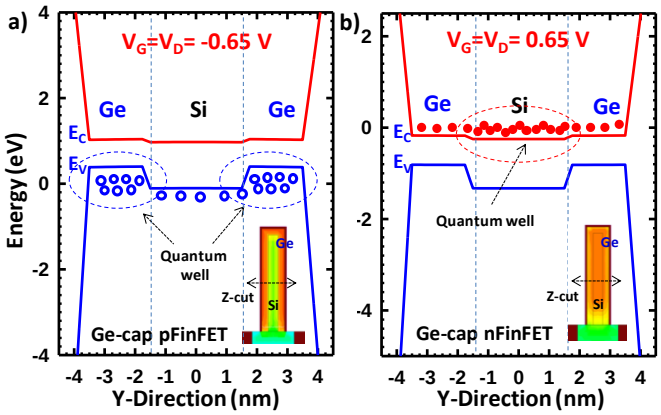

Fig. 4 Band diagram of simulated Ge-cap QW a) pFinFET and b) nFinFET under on-state condition ($|V_D|$=$|V_G|$=0.65V)

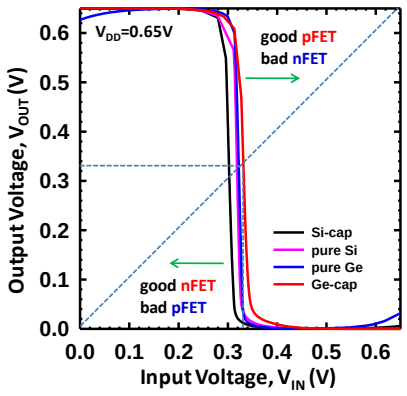

Fig. 5 Comparison of voltage transfer characteristics (VTC) of pure Si, pure Ge, Si-cap, and Ge-cap FinFET CMOS inverter with V_{DD}=0.65V

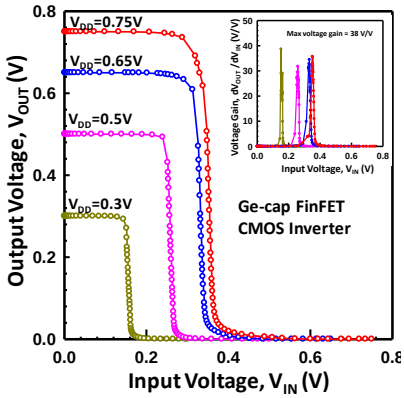

Fig. 6 Voltage transfer characteristics (VTC) of Ge-cap QW FinFET CMOS inverter with highest gain 38V/V

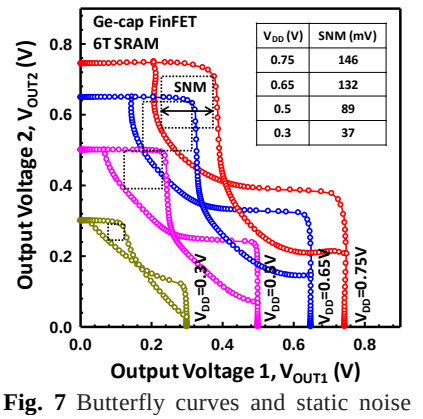

Fig. 7 Butterfly curves and static noise margin (SNM) values of Ge-cap QW FinFET 6T SRAM cells during read access