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TCAD simulation of planar single-gate Si tunnel FET with average subthreshold swing less than 60 mV/dec for 0.3 V operation

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Abstract

TCAD simulations have been performed to optimize well designed planar single-gate silicon (Si) vertical tunneling junction field effect transistor (VTFET) with average subthreshold swing (S.S.) less than 60 mV/dec for 0.3 V (=*V*gs=*V*ds) operation. By scaling the equivalent oxide thickness (EOT) and increasing the gate-to-source overlap length *L*ov, it achieved both on-current (*I*on) greater than 1.0 μA/μm and low average S.S. without pocket doping for forming tunnel junction in conventional VTFET.

1. Introduction

With lower S.S. below the MOSFET thermal limit (60 mV/dec at 300 K), tunnel field effect transistor (TFET) is attracting interest for ultra-low power operation. By forming the pocket region with polarity opposite to the source region in the planar single-gate Si TFET as shown in Fig. 1, it is possible that steep S.S. less than 60 mV/dec has been achieved due to uniform source-to-pocket band-to-band tunneling (BTBT) turn-on voltage in previous works [1]. However, source-pocket junction depth needs to be ultra shallow which requires very difficult low energy implantation process [2].

In this work, we optimized the structure of Si VTFET for high *I*on and low S.S. by using TCAD simulations. The optimum impurity profile and the necessity of pocket implantation are discussed.

2. Device Structure and Bias Condition

The calculated device structures are n-type VTFETs, where tunneling takes place in the junction between the p+ source region and n- pocket region. Figures 2 (a) and (b) show typical impurity profiles of donor and acceptor, respectively. The devices are assumed to consist of rectangle materials for simplicity. Applied gate-to-source voltages V_{gs} are sweeping from 0.0 to 0.3 V, whereas drain-to-source voltages V_{ds} are fixed to 0.3V. Metal work function of gate electrode is adjusted that the voltage at which the current begins to increase is 0V. We defined *I*on as the drain current at V_g=0.3 V. The average S.S. between V_g = 0 V and V_g = 0.3 V is evaluated.

3. Results and Discussion

Figure 3 shows the one of the simulation results of VTFET I-V characteristics which have ave. S.S. less than 60 mV/dec. For the low S.S. (< 60 mV/dec), it is necessary that the pocket concentration is lower than the source concentration as shown in Fig. 4(a). The reason is that high pocket concentration (N_A~N_D) leads to source-to-pocket BTBT current in off state, which causes the pocket-to-drain thermal diffusion current (Fig. 4 (c)).

While satisfying this condition, the impurity concentration (source and pocket) dependences of *I*on and ave. S.S. are investigated as shown in Fig. 5. In order to obtain both high *I*on and low ave. S.S., it is necessary to avoid too-low pocket concentration on the condition that the EOT of gate dielectric layer is 2.0 nm. You can find that the concentrations to fulfill the requirements for ave. S.S. less than 60 mV/dec enable to obtain the high *I*on at the same time. However, when EOT is 0.29nm, both ave. S.S. and *I*on are improved overall (Fig. 6). These come from the enhanced electrical coupling between the gate electrode and the source-to-pocket tunnel junction due to high gate capacitance, which increases the BTBT rate [3]. 0.29 nm of EOT is equivalent to relative dielectric constant ~ 27 [4] for 2.0 nm gate insulator. In Fig. 6, the condition that meets both low S.S. (< 60 mV/dec) and high *I*on is different from that in Fig. 5. Here it should be noted that we don’t need to keep the certain amount of pocket concentration. It indicates that VTFET without the pocket (pocketless) could achieve the good characteristics in the case of EOT = 0.29 nm. Figure 7 shows the simulated EOT dependence of ave. S.S. and *I*on, which compares the conventional VTFET (with pocket) and pocketless VTFET. Note that the discrepancy between the two is decreased as EOT is made thinner, and especially at the EOT = 0.29 nm, pocketless VTFET has the same characteristics as VTFET with pocket.

For the further improvement, the gate stack to source overlap length *L*ov is increased, which simply contribute to expansion of tunneling area (Fig. 8). Figure 9 is the simulated I-V characteristic of pocketless VTFET with EOT = 0.29 nm and increased *L*ov (= 0.38 μm). The detailed extracted electrical characteristics and device parameters are shown in Figs. 9 (a) and (b), respectively.

3. Conclusions

We have investigated the ave. S.S. and *I*on of Si VTFET with pocket implantation for V_{gs}=V_{ds}=0.3 V by using TCAD simulation. In the case of thin EOT, it has indicated that pocketless VTFET is expected to have the same performance as VTFET with pocket shown in past reports. Furthermore, it is understood that expanded gate to source overlap simply improves the characteristics. Pocketless VTFET has a significant advantage that there is no need to use the very difficult shallow and steep implantation process including concerns about manufacturing fluctuations.

Acknowledgements

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References

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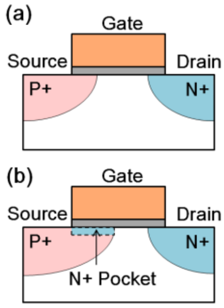


Fig. 1. Schematic diagrams of (a) conventional Si TFET and (b) Si vertical TFET.

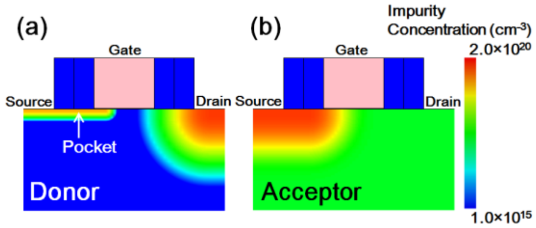


Fig. 2. Simulated device shape and impurity profiles of vertical Si VTFET. (a) Donor and (b) acceptor.

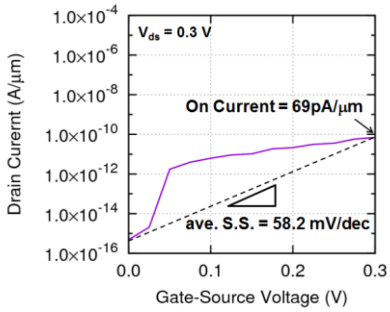


Fig. 3. Simulated I-V result of Si VTFET with ave. S.S. less than 60 mV /dec.

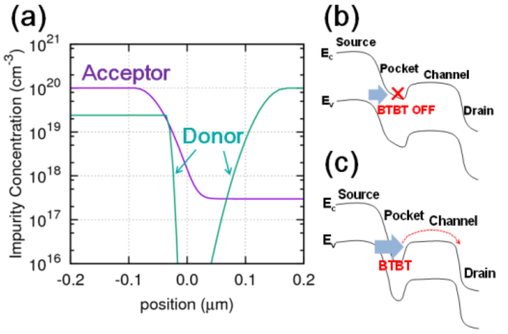


Fig. 4 (a) Impurity profile of simulated structure with S.S. less than 60 mV/dec at Si surface and schematic off state band diagram along with current conduction path ((b) $N_A>N_D$ and (c) $N_A\sim N_D$).

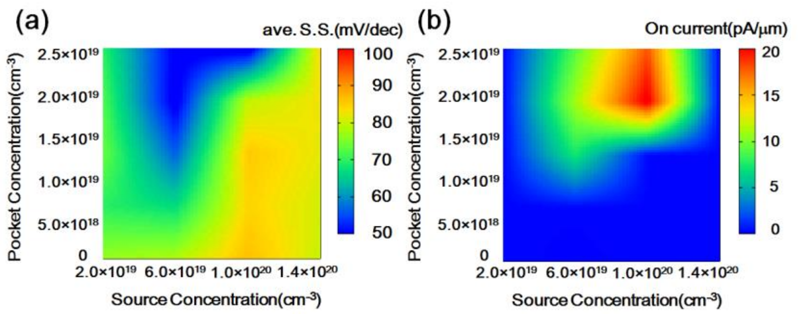


Fig. 5. Simulated pocket concentration and source concentration dependence of *I*on and S.S. with EOT = 2.0nm.

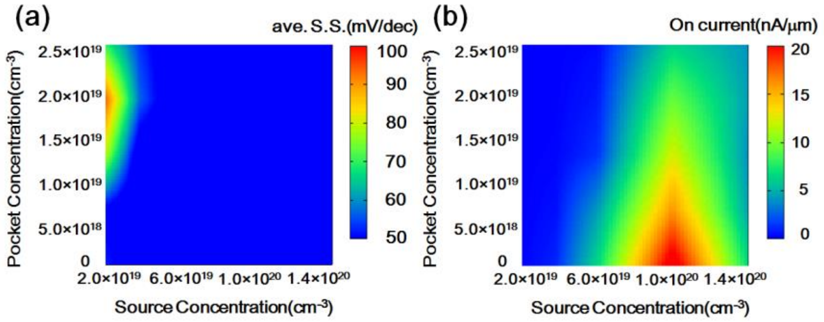


Fig. 6. Simulated pocket concentration and source concentration dependence of *I*on and S.S. with EOT = 0.29 nm.

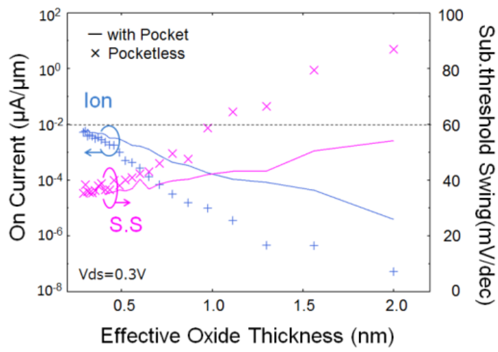


Fig. 7. Comparison of simulated EOT dependence of *I*on and S.S. of Si VTFETs with pocket and pocketless. *L*ov = 0.03 µm.

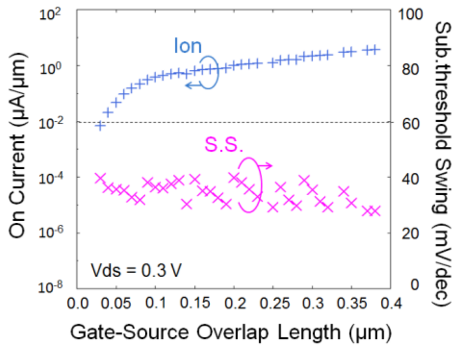
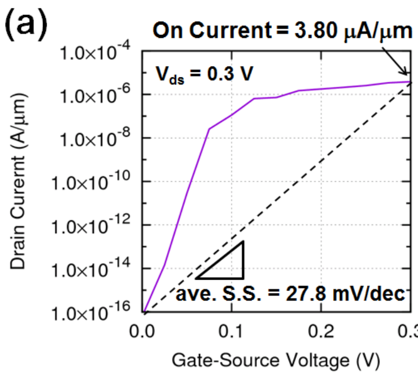


Fig. 8. Simulated *L*ov dependence of *I*on and S.S. with EOT = 0.29 nm.



(b)

Parameter	
EOT	0.29 nm
Lov	0.38 µm
Source Concentration	5.5×10^{19} cm^{-3}
Drain Concentration	1.0×10^{20} cm^{-3}

Fig. 9. (a) Simulated I-V curve of pocketless Si VTFET with *L*ov = 0.38 µm and EOT = 0.29 nm, and (b) the list of detailed device parameters.