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Low-Temperature Microwave Annealing Process for $In_{0.53}Ga_{0.47}As$ MOSFETs

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Abstract

We propose the microwave annealing (MWA) as a low thermal budget source/drain (S/D) formation process in activating the implanted dopants for the $In_{0.53}Ga_{0.47}As$ MOSFETs. Compared to the conventional rapid thermal annealing (RTA), the MWA provides lower contact resistance (108.7 Ω-μm), contact resistivity ($8.25x10^{-7}$ Ω-cm^2) and sheet resistance (144.57 Ω/□) extracted from the transmission line model (TLM) test structures. In addition, the MWA InGaAs MOSFET device exhibits the improved on-state current (I_{DS} = 85.6 μA/μm at V_{GS} = 2 V), transconductance (G_m = 45.42 μS/μm), and suppresses the off-state current by more than 5 times.

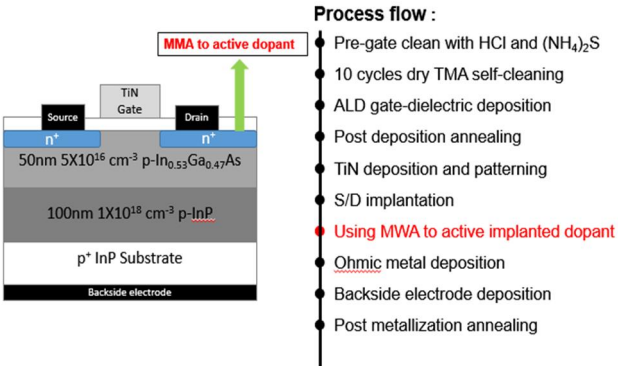
1. Introduction

The integration and the performance of complementary metal-oxide-semiconductor (CMOS) devices have been improved considerably through continual device size shrinking. One of the key technical challenges is to form the heavily doped source/drain (S/D) regions with ultra-shallow depths [1]. To obtain a low contact resistance with a small junction leakage, conventional rapid thermal annealing (RTA) have been performed in order to activate the implanted dopants and repair partly the lattice damages caused by ion implantation process. However, high-temperature RTA process results in high dopant diffusion that restricts the good S/D junction formation. This issue becomes more serious when the high mobility materials have emerged as the alternative channel to replace Si-based materials in future electronic applications. Due to their low dopant solid solubility and high diffusivity, the suppression of the series resistance is challenging, especially in the case of III-V compound semiconductor materials. In this article, we examine the low thermal budget MWA process in the S/D formation and demonstrate electrical characteristics of successful fabrication of $In_{0.53}Ga_{0.47}As$ MOSFETs utilizing this approach.

2. Experimental Procedure

The epitaxial structure used in this study consisted of 50 nm p-$In_{0.53}Ga_{0.47}As$ (5 x 10^{16} Be doped) channel layer and 100 nm p^+-InP buffer layer on the p^{++}-InP substrate grown by solid source molecular beam method as the starting material. First, to evaluate the influences of MWA process on the dopant activation, the n^+/p junction, and TLM test structures were fabricated by using implantation with Si^+ ions (15 keV, 1×10^{14} cm^{-2}) and different MWA processes (2100-3000 W, 100-300 sec). Next, the gate-first self-aligned process was used to fabricate the $In_{0.53}Ga_{0.47}As$ MOSFETs as can be seen in Fig. 1. After degreasing in acetone and isopropanol, the chemical pretreatments were carried out by 4% HCl solution for 2 minutes followed by 10% $(NH_4)_2S$ solution for 20 minutes. Then, a 10-nm Al_2O_3 was deposited as the gate oxide by Atomic Layer Deposition (ALD) at 250˚C. After that, post deposition annealing (PDA) was performed at 400˚C for 2 minutes in forming gas. A 100 nm-TiN metal gate electrode was deposited by physical vapor deposition. Gate pattern was defined via optical lithography and TiN dry-etching was conducted using inductively coupled plasma reactive ion etching. The S/D formation was done using the optimized MWA condition. Au/Ge/Ni/Au S/D ohmic and AuBe backside contact were formed by e-beam evaporation, and post metallization annealing was finally performed at 300˚C in 30 seconds in N_2. The $In_{0.53}Ga_{0.47}As$ MOSFET with the conventional RTA process was also accomplished for comparison.

Fig. 1 Schematic diagram of device structure and process flow for the $In_{0.53}Ga_{0.47}As$ MOSFET fabrication with MWA.



3. Results and Discussion

Fig. 2(a) shows the current-voltage (*I-V*) characteristics of the silicon doped n^+-$In_{0.53}Ga_{0.47}As$/p-$In_{0.53}Ga_{0.47}As$ diodes fabricated with MWA process at the power of 2400 W for various annealing times. Good rectifying behaviors were observed with the forward/reverse currents were approximately 6 orders of magnitude. In Fig. 2(b), the effective barrier height and ideality factor were evaluated from the power and annealing time dependence of the forward current in the n^+-$In_{0.53}Ga_{0.47}As$/p-$In_{0.53}Ga_{0.47}As$ diodes. It is revealed that the MWA process with a power of 2400 W for 200 seconds provided an effective barrier height of 0.68 eV and small ideality factor ~ 1, which was beneficial in restraining the leakage current and improving device performance.

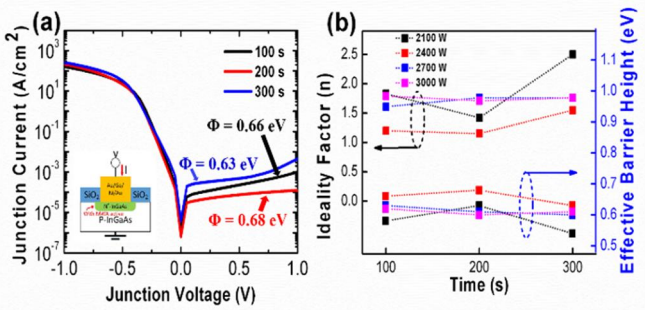


Fig. 2 (a) *I-V* electrical characteristics of n^+-$In_{0.53}Ga_{0.47}As$/p-$In_{0.53}Ga_{0.47}As$ diodes with at MWA power of 2400 W for different annealing durations. The inset in (a) shows the schematic illustration of the junction cross section. (b) Ideality factor and effective barrier height with a variety of MWA conditions.

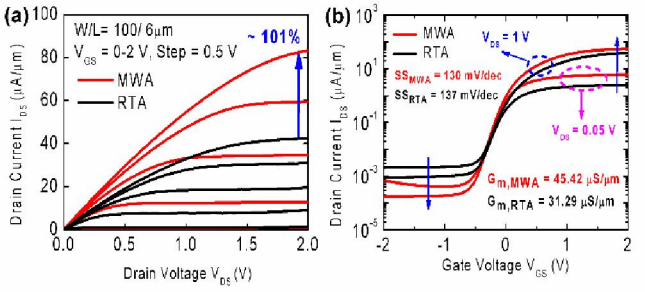


Fig. 3 (a) Output and (b) transfer characteristics of InGaAs MOSFETs fabricated with MWA and RTA processes.

The output characteristics of the $In_{0.53}Ga_{0.47}As$ MOSFET with gate length (L_G) of 6 μm and gate width (W_G) of 100 μm are shown in Fig. 3(a). The MWA device provided 101% drive current enhancement as compared to the RTA device. This device shows I_{DS} of 85.6 μA/μm at V_{GS} = 2 V and V_{DS} = 2 V. Besides, the MWA device has high on/off ratio of ~ 10^5, SS of 130 mV/dec, and $G_{m,max}$ of 45.42 μS/μm. The MWA device shows an I_{off} lower more than 5 times as compared to the RTA device. It is reasonable that MWA, owning to its selective heating effect and low-temperature annealing, helped to create a good S/D formation with the suppressed junction extension or diffusion phenomenon.

Fig. 4(a) and (b) plot the on-resistance R_{on} in the linear regime (V_D = 0.1 V) as a function of L_G at three gate voltage of 1, 1.5 and 2 V. The fitted curves were extrapolated to show

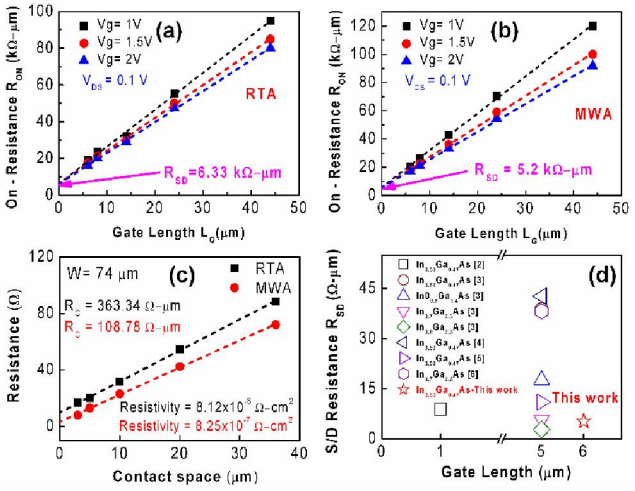


Fig. 4 Total resistance as a function of gate length for (a) RTA and (b) MWA samples. (c) TLM resistance versus spacing gap for RTA and MWA samples. (d) Benchmark S/D resistance of this work with reported values [2-6] on the InGaAs MOSFETs.

an intersection point. The intercept shows the R_{SD} of ~ 6.3 kΩ-μm and 5.2 kΩ-μm for RTA and MWA devices, respectively. From TLM resistance in Fig. 4(c), the contact resistance (R_C) and the sheet resistance (R_{sheet}) were extracted by the intercept of linear fitting line with the vertical axis and the slope of the fitting line, respectively. Resistivity is equal to R_C times transfer length (L_T) and gate width (W). Compared to the RTA device, the MWA device shows lower R_C of 108.78 Ω-μm, R_{sheet} of 144.57 Ω/□, and resistivity of 8.25×10^{-7} Ω-cm^2. Fig. 4(d) shows that this work obtains lowest source/drain series resistance among the InGaAs MOSFETs with the In content of 0.53.

3. Conclusions

We report the $In_{0.53}Ga_{0.47}As$ MOSFETs utilizing low-temperature MWA process to activate the implanted dopants for S/D formation. Better electrical characteristics and lower contact resistance, sheet resistance, and resistivity were demonstrated as compared to the InGaAs MOSFET activated by conventional RTA process. The achieved results in this work prove that MWA technique is promising for the future low power consumption and high performance applications.

Acknowledgements

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