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Role of Al_2O_3 Thin Layer to Improve The Switching Properties in Ta_5Si_3 Based CBRAM Device

Dayanand Kumar, Rakesh Aluguri, Sridhar Chandrasekaran, Umesh Chand and Tseung-Yuen Tseng*
Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 30010,Taiwan,
*E-mail: tseng@cc.nctu.edu.tw

Abstract

The switching properties of the Ta_5Si_3 based CBRAM device are investigated for nonvolatile memory applications. The resistive switching properties can be improved by inserting a thin Al_2O_3 layer between the bottom electrode and Ta_5Si_3 layer. The Ta_5Si_3/Al_2O_3 double layer device with the 1 nm thin Al_2O_3 layer exhibits excellent memory performances, such as stable DC endurance up to 10^4 cycles during the test without degradation, good retention ability (>10^5 s) at a temperature of 130^{0}C with more than 10^2 resistance ratio.

1. Introduction

Conductive Bridge RAM (CBRAM) has been considered to be a promising candidate to replace NAND FLASH memory because of its high scalability, high retention, large memory window and low power consumption [1-3]. The resistive switching (RS) principle in a CBRAM device is based on the formation and rupture of the conductive filaments consisting of oxidation and reduction of metal (Cu+, Ag+) ions [4]. Bilayer based CBRAM devices are found to be exhibiting better memory characteristics such as stable switching voltages, on/off ratio, compared to the single layer devices by controlling the conducting filament (CF) size and position [5,6]. In this study, we investigate double layer CBRAM device with the insertion of an Al_2O_3 layer between Ta_5Si_3 layer and bottom electrode to control the formation and rupture of the conductive filament, which shows highly stable switching characteristics with narrow fluctuations in set/reset voltages.

2. Experimental Detail

A 20 nm thick Ti adhesion layer and a 50 nm thick Pt bottom electrode (BE) were deposited by electron beam evaporation on SiO_2/Si substrate. Al_2O_3 of thickness 1 nm, 3 nm and 5 nm were deposited on Pt BE by atomic layer deposition and then 10 nm thick Ta_5Si_3 was deposited by a radio-frequency (RF) magnetron sputtering at room temperature. Finally, 4 nm Ta and 250 nm thick Cu top electrode were deposited by sputtering to form Cu/Ta/Ta_5Si_3/Al_2O_3/Pt double layer CBRAM structure.

3. Result and Discussion

The cross-sectional TEM image of the Cu/Ta/Ta_5Si_3/Al_2O_3/Pt double layer device are illustrated in Fig.1. The TEM image shows the clear and distinguished presence of various layers within the device. It confirms that the double layer device consists of Cu top electrode, 4 nm Ta adhesion barrier layer, 10 nm Ta_5Si_3 switching layer, 1-nm Al_2O_3 interfacial layer between Ta_5Si_3 and Pt BE. The typical forming process and DC sweep I-V curve of the single layer (SL) and double layer (DL) devices are shown in Fig-2, where both devices are showing bipolar resistive switching behavior. Fig-3 compares the distribution of resistance in HRS and LRS states during continuous switching upto 1000 sweep cycles. Significant fluctuations of both HRS and LRS are observed in the SL device, while it shows the narrower distribution in the DL device. Obviously, the uniformity of LRS and HRS can be improved by inserting a thin Al_2O_3 layer between the Ta_5Si_3 layer and BE. It indicates that the stochastic formation and rupture of CF in the SL device while the effective RS region is confined in the DL device at Al_2O_3/Pt interface so that the DL device possesses sharp distributions in LRS and HRS, leading to the stable RS characteristics. The RS characteristics of SL device and DL devices with different Al_2O_3 thicknesses are shown in Fig. 4. On the other hand, the wide fluctuations of the resistance in DL devices with 3 nm and 5 nm Al_2O_3 compared to that of 1 nm Al_2O_3 DL device are observed during continuous switching as shown in Fig. 5. This phenomenon is caused by the random formation and rupture of the conductive filament in the thicker Al_2O_3 film, which suggests that the region for rupture of the conductive filament is large. Fig. 6 and Fig. 7 show the DC endurance test for all devices which can well maintain its states for more than 10^4 cycles without any degradation in DL device with Al_2O_3 1 nm thickness. The non-volatility of data storage is further confirmed by retention test measured at 130^{0}C. The DL device shows good retention property at high temperature for more than 10^5 s, as shown in Fig. 8.

4. Conclusion

The switching characteristics and uniformity of the Ta_5Si_3 based CBRAM device has been extremely enhanced with inserting a thin Al_2O_3 layer between Ta_5Si_3 and BE. Enhanced on/off resistance ratio (>10^2) and endurance of (>10^4) is achieved without any degradation in the DL device due to the control of the formation and rupture of the CF at Al_2O_3/Pt interface. The two resistance states are stable over 10^5 s at 0.3 V without any observable degradation at 130^{0}C, which demonstrates the good reliability of the DL device at higher temperature. These results indicate that the RS properties of the Ta_5Si_3 based device have been improved by inserting the 1 nm thin Al_2O_3 layer.

Acknowledgement

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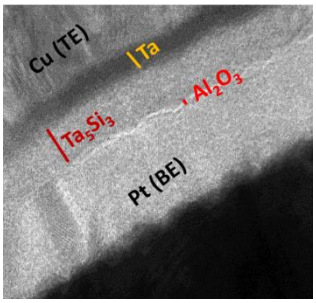

Fig.1 Cross-sectional TEM image of Cu/Ta/Ta_5Si_3/Al_2O_3/Pt device.

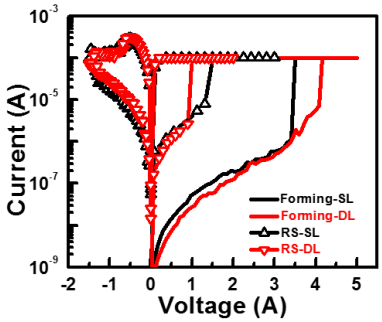

Fig.2 Forming process and I-V switching curves of the SL and DL devices.

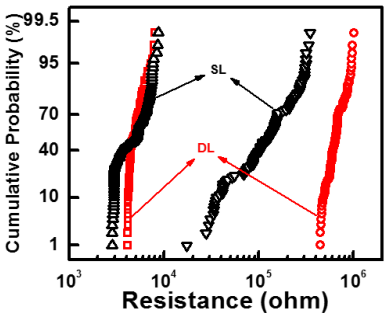

Fig.3 Distribution of resistances in HRS and LRS for 1000 sweep cycles.

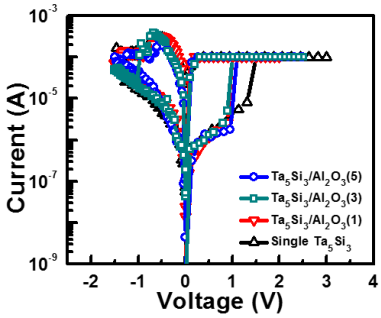

Fig.4 I-V switching curves of single Ta_5Si_3 device and with Al_2O_3 thickness (from 1nm to 5 nm)

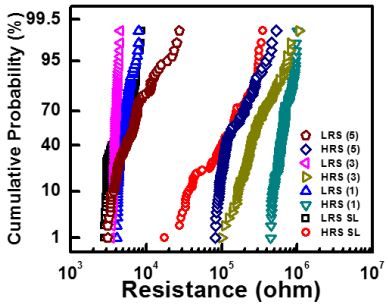

Fig.5 Distribution of resistances in HRS and LRS for 1000 sweep cycles for SL and DL devices.

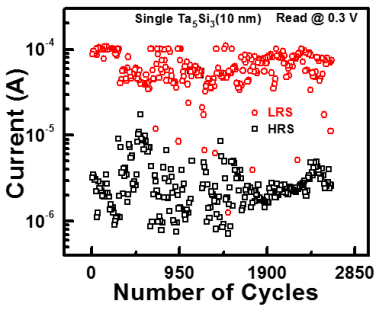

Fig.6 (a) Endurance test for SL devices measured at room temperature.

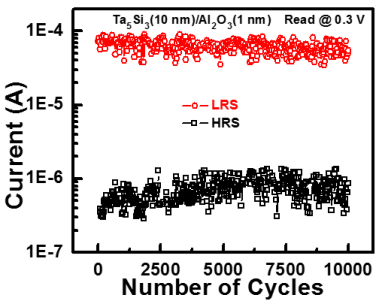

Fig.6 (b) Endurance test for DL devices measured at room temperature.

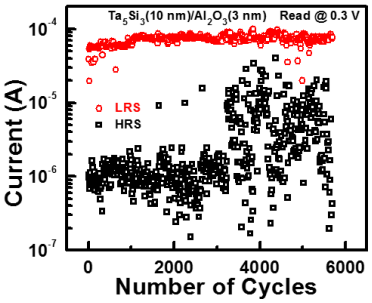

Fig.7 (a) Endurance test for DL device with Al_2O_3 3 nm thickness measured at room temperature.

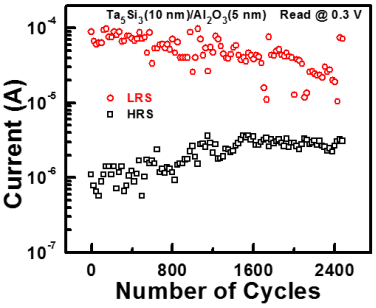

Fig.7 (b) Endurance test for DL device with Al_2O_3 5nm thickness measured at room temperature.

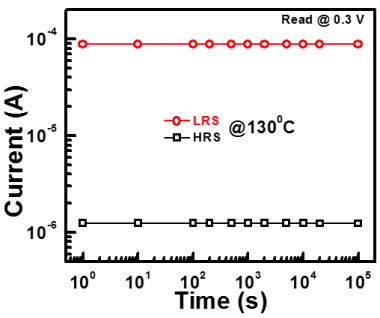

Fig.8 Retention behavior measured at temperature of 130^{0}C for DL device.