PS-4-06

Error-Correction & Set/Reset Verify Strategy of Storage Class Memory (SCM) for SCM/NAND Flash Hybrid and All-SCM Storage

Chihiro Matsui and Ken Takeuchi
Chuo University, 1-13-27 Kasuga, Bunkyo-ku, Tokyo 112-8551, Japan, E-mail: matsui@takeuchi-lab.org

Abstract

Error-correction and set/reset verify strategy of storage class memory (SCM) in SCM/NAND flash hybrid storage and all-SCM storage is proposed. With read-intensive application, strong ECC should be applied to the hybrid storage while SCM cell errors in the all-SCM storage are corrected by set/reset verify and weak ECC.

1. Introduction

As shown in Fig. 1, storage with storage class memory (SCM) can take two forms: (a) SCM/NAND flash hybrid [1] and (b) all-SCM storage [2]. The hybrid storage is used as Tier 1-2 storage in data center to store/manage wide variety of data. Dominant application of in-memory database is read-intensive which requires short latency. Thus, the all-SCM storage can be used as an alternative to DRAM. Because of different access volume to SCM, error correction and set/reset verify strategy should be changed with storage organization and also application characteristics.

2. Error Correction and Set/reset Verify of SCM

Fig. 2 shows candidates of SCM [3-6]. These SCMs have different characteristics because of their switching mechanisms such as 50 ns reset time of ReRAM (Fig. 3(a)) [7]. In addition, cell bit error rate (BER) in SCM increases with set/reset cycles (Fig. 3(b)) [8]. Errors in SCM can be reduced by set/reset verify operation and/or corrected by error correcting code (ECC). In our previous work, only ECC is applied to correct errors in the hybrid storage [9], and the all-SCM storage changes set/reset verify to ECC with increased SCM set/reset cycles [10].

In SCM, set/reset verify operation repeats program pulse and verify-read until program successes (Fig. 4(a)). As shown in Fig. 4(b), program BER is reduced by 49% with 20 verify cycles [11] while the cell program time becomes 20 times longer. Total SCM cell program time t_{PROG} becomes long with more verify cycles, N_{verify} by the following Eq. 1.

$$\text{SCM } t_{PROG} = (t_{SET/RESET} + t_{READ}) \times N_{verify} \quad (1)$$

In this work, both $t_{SET/RESET}$ and t_{READ} are assumed as 50 ns, and N_{verify} =1 when no verify operation is operated.

Bose-Chaudhuri-Hocquenghem (BCH) code is applied to correct random errors in SCM [2]. Here, the user data of SCM is the sector, 512 Byte. Based on [12, 13], encoding/decoding time of (*n, k, t*) BCH code in Fig. 5(a) are calculated with

$$t_{ECC\ encode} = n(F \times p) \quad (2)$$

$$t_{ECC\ decode} = \{mt/p + (t+1)f/2 + n/p\}/F. \quad (3)$$

Here, n is the codeword, k is the user data size, t is the predetermined correctable bits, m is the order of Galois field GF(2^m), p is the number of parallelism, f is the folding factor, and F is the operation frequency. As shown in Fig. 5(b), ECC encoding/decoding time and the acceptable BER increases as the error correction capability increases. In particular, the SCM read time including cell reading and ECC decoding becomes longer. Thus, set/reset verify and ECC increase the program and read time, respectively. From the system viewpoint, the impact on storage performance by set/reset verify and ECC depends on the storage organizations, that is, hybrid or all-SCM, and the application characteristics such as write-intensive or read-intensive.

3. Storage Algorithm and Evaluation Results

Three program BER of SCM without set/reset verify, $BER_{baseline}$, is assumed as listed in Table I [2]. If set/reset verify of SCM is operated, the program BER is reduced from $BER_{baseline}$ according to three scenarios in Fig. 6 [2], and required ECC capability is reduced. In the scenarios, one verify operation is assumed to reduce the program BER by half, and $BER_{baseline}$ is converged to 1/2, 1/10, and 1/100 with N_{verify}. Note that NAND flash requires BCH ECC capability with 9/10 code rate to correct 428 bit errors in 8 KByte user data. To evaluate storage performance, a transaction-level modeling based emulator is used [1] with SCM and NAND flash characteristics listed in Table II [14]. Write/read-intensive prxy_0 or prxy_1 [15] is input as a workload of the emulator. Data management algorithm of the hybrid storage utilizes cold data eviction [1] with 1%, 3%, and 10% SCM capacity of NAND flash. Unlike [2], the parity bits for SCM and NAND flash are stored in the correspondent memory devices.

Figs. 7 and 8 compare storage performance of (a)-(c) hybrid and (d) all-SCM storage with prxy_0 and prxy_1. IOPS performance of the hybrid and all-SCM storage are improved compared to NAND flash only storage. However, set/reset verify and ECC operations degrade the performance. Moreover, the performance degradation trends are different, depending on the storage organization and application characteristics. Because prxy_0 is write-intensive, set/reset verify increases program time of SCM with any $BER_{baseline}$ case, and degrades performance of both the hybrid (Fig. 7(a)-(c)) and the all-SCM storage (Fig. 7(d)). With read-intensive prxy_1 (Fig. 8), the strategy of SCM is different in the storage organization and SCM capacity. Set/reset verify improves the performance by upto 23% for the hybrid storage with 1% SCM capacity (Fig. 8(a)) and 40% for all-SCM storage (Fig. 8(d)). Instead, the performance of the hybrid storage with 5% and 10% SCM capacity (Figs. 8(b) and 8(c)) increases by only 7% with set/reset verify. Since SCM $t_{ECC\ decode}$ is reduced by 46% with weak ECC, the total time does not change even if SCM t_{PROG} becomes 5 times longer. The performance difference between the hybrid and all-SCM storage is explained with Fig. 9. The performance degradation rate of verify cycles and ECC correctable bits are 2.1 times and 3.6 times less sensitive in the hybrid storage than the all-SCM storage. In more detail, one verify cycle degrades the performance by 7.8×10^{-3} for the hybrid storage and 1.6×10^{-2} for the all-SCM storage. In addition, if the required ECC correctable bits is reduced by 1 bit, the storage performance is increased by 4.2×10^{-3} for the hybrid storage and 1.5×10^{-2} for the all-SCM storage. This means that the set/reset verify contributes less to the performance of the hybrid storage in both write-intensive and read-intensive applications. Therefore, set/reset verify improves the performance of the all-SCM storage more than the hybrid storage.

4. Conclusions

Table III summarizes error correction and set/reset verify strategy of SCM in the hybrid and all-SCM storage. Strong ECC with fast SCM programming is preferred for both write/read-intensive applications in the SCM/NAND flash hybrid storage with SCM capacity 10%. In contrast, the strategy of the all-SCM storage is switched from strong ECC with fast program for the write-intensive application to weak ECC with 5 verify cycles for the read-intensive application.

Acknowledgements This work is partly supported by NEDO.

References [1] C. Sun et al., *TCAS-I*, vol. 61, no. 2, pp. 382-392, 2014. [2] H. Takishita et al., *NVMW*, 2017. [3] S.-W. Chung et al., *IEDM*, 2016, pp. 27. [4] K. Kawai et al., *ICICDT*, 2014, pp. 100-103. [5] Y. Choi et al., *ISSCC*, 2012, pp. 46-48. [6] Micron 3D XPoint Technology, https://www.micron.com/about/our-innovation/3d-xpoint-technology. [7] S. Ning et al., *IMW*, 2013, pp. 56-59. [8] K. Maeda et al., *IRPS*, 2017, pp. 5A-4. [9] H. Takishita et al., *SNW*, 2015, pp. 3-4. [10] A. Hayakawa et al., *IMW*, 2017, pp. 24-27. [11] S. Ning et al., *Jpn. J. Appl. Phys.*, vol. 53, no. 4S, pp. 04ED09, 2014. [12] H. Tang et al., *ISCAS*, 2015, pp. 1997-2000. [13] Y. Lee et al., *ISSCC*, 2012, pp. 426-428. [14] C. Matsui et al., *SSDM*, 2016, pp. 105-106. [15] MSR Cambridge Traces, http://iotta.snia.org/traces/388.

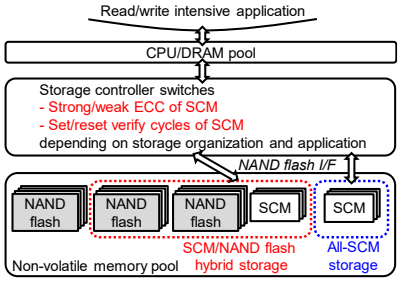

Fig. 1 Proposed storage system architecture. ECC and set/reset verify strategy of SCM are switched for SCM/NAND flash hybrid and all-SCM storage with application characteristics.

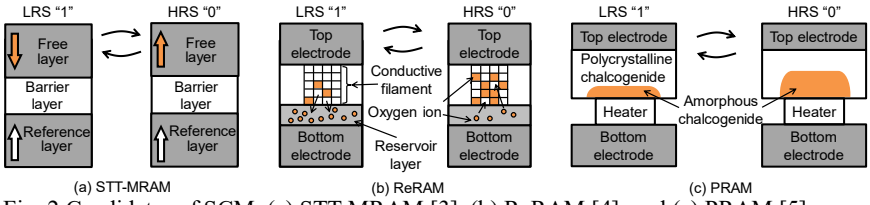

Fig. 2 Candidates of SCM. (a) STT-MRAM [3], (b) ReRAM [4], and (c) PRAM [5].

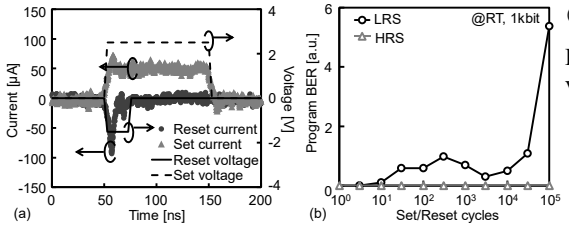

Fig. 3 (a) Measured set/reset time [7] and (b) BER [8] of ReRAM.

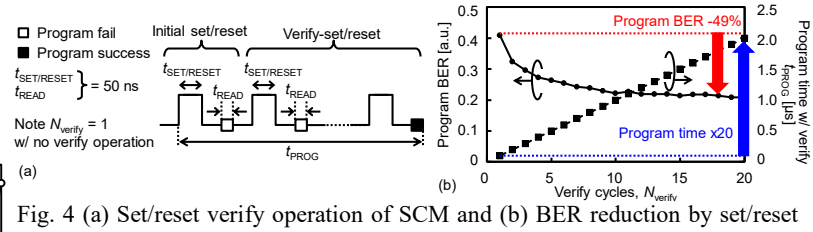

Fig. 4 (a) Set/reset verify operation of SCM and (b) BER reduction by set/reset verify [11].

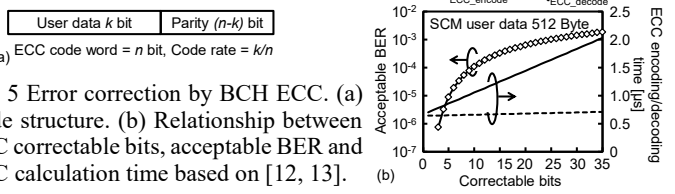

Fig. 5 Error correction by BCH ECC. (a) Code structure. (b) Relationship between ECC correctable bits, acceptable BER and ECC calculation time based on [12, 13].

Table I
Baseline BER assumption of SCM w/o set/reset verify [2]

	SCM Baseline BER (w/o verify)	Required correctable bits
Case 1	1.9×10^{-3}	35 bit
Case 2	6.1×10^{-4}	20 bit
Case 3	1.1×10^{-4}	10 bit

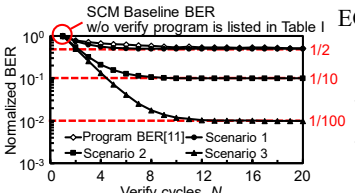

Fig. 6 Three BER reduction scenarios by set/reset verify [2, 11].

Table II
Memory characteristics for evaluation [14]

Memory device	Read time	Program time	Erase time	I/O frequency	V_{DD} (Core, I/O)	Access unit
SCM	0.05 us/sector	Eq. 1	Not required	1066 MHz	1.8V, 1.2V	Sector (512Byte)
MLC NAND flash	52 us/page (U) 36 us/page (L)	2000 us/page (U) 370 us/page (L)	3300 us/block	400 MHz	3.3V, 1.8V	Page (16KByte)

U: Upper page, L: Lower page of MLC NAND flash

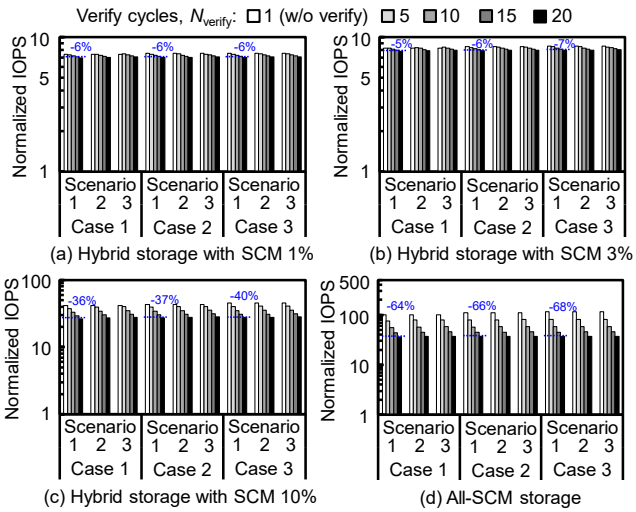

Fig. 7 Storage performance with write-intensive prxy_0. Errors in SCM are corrected by BCH ECC after set/reset verify operation.

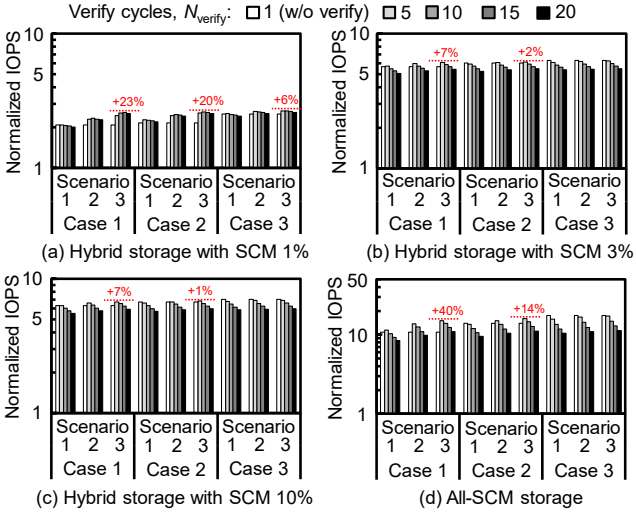

Fig. 8 Storage performance with read-intensive prxy_1. Errors in SCM are corrected by ECC after set/reset verify operation.

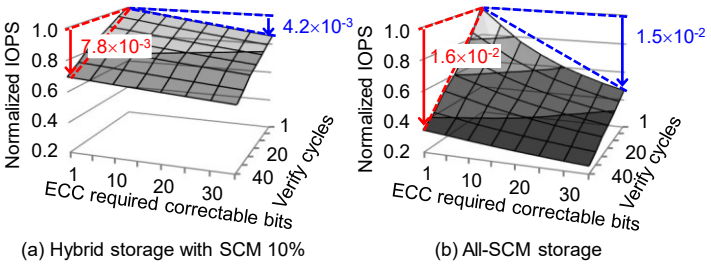

Fig. 9 Performance degradation by set/reset verify and BCH ECC. (a) Hybrid storage with SCM 10% and (b) all-SCM storage.

Table III
Summary of this work

w/ Case 1, Scenario 3

Application	SCM/MLC NAND flash hybrid storage w/ 10% SCM capacity	All-SCM storage
write-intensive (prxy_0)	Strong ECC w/ fast program (No set/reset verify)	Strong ECC w/ fast program (No set/reset verify)
read-intensive (prxy_1)	Strong ECC w/ fast program (No set/reset verify) or Weak ECC w/ 5 verify cycles	**Switch strategy** Weak ECC w/ 5 verify cycles ⇒ 40% performance improvement by verify