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Impacts of Low Temperature formed SiO_2 Tunneling and Si_3N_4/HfO_2 Trapping Layers on Gate-All-Around Charge-Trapping Flash Memory Devices

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Abstract

Low temperature (LT) formed SiO_2 tunneling and Si_3N_4/HfO_2 trapping layers on operation characteristics of gate-all-around (GAA) charge trapping flash devices were studied. Devices with Ω-nanowire configuration were also compared. Faster operation speeds and larger memory windows are achieved by GAA configuration. However, worse retention characteristics of GAA devices may be caused by less coverage of LT formed SiO_2 and Si_3N_4 layer. The coverage issue of LT deposited dielectrics should be resolved to be implemented on GAA CT flash devices for 3D memory appliactions.

1. Introduction

Polycrystalline silicon (Poly-Si) channel has been widely applied on flash devices for three-dimensional (3D) memory integration due to the fast increasing demand of non-volatile memory market. Recently, gate-all-around (GAA) configuration was widely applied on charge-trapping (CT) flash devices, indicating that operation characteristics can be much improved by GAA configuration [1]. Furthermore, stacked trapping layer such as Si_3N_4/high-k was reported to enhance the operation characteristics of CT flash devices [2]. However, thermal budget of fabrication process should be reduced and carefully controlled due to increased vertical layer of channel architecture and application of high-k dielectrics in 3D flash devices. In this work, low temperature (LT) formed SiO_2 tunneling and stacked Si_3N_4/HfO_2 trapping layers on operation characteristics of CT flash device with GAA and Ω-gate nanowire (NW) configurations were studied.

2. Device Fabrication

Poly-Si GAA and Ω-gate NW devices were fabricated on 6-inch Si wafers. For GAA devices, a 100-nm thick SiO_2, a 50-nm thick Si_3N_4 buried layer, a 100-nm thick tetraethoxysilane (TEOS) oxide and a 100 nm thick in-situ n-doped poly-Si were sequentially deposited by low pressure chemical vapor deposition (LPCVD). Then, all samples were sent to form active region of suspend poly-Si channel by the following processes. In-situ poly-Si layer was patterned and etched to form four mesa stripes with a height of 70 nm. A 50-nm thick Si_3N_4 was then deposited by LPCVD and carefully etched to leave sidewall spacers around mesa stripes. S/D pads were defined and reactive-ion etching (RIE) process was performed to remove the exposed poly-Si layer. The poly-Si channels were formed by the protection of Si_3N_4 spacer, and they were connected with S/D pads. Afterwards, the spacer was removed by phosphoric acid (H_3PO_4). The TEOS oxide under poly-Si channels was then remove by diluted HF to complete active region formation. As for the Ω-gate NW devices, the formation of active region is similar to that in [3]. Next, a 3-nm thick tunneling oxide was grown by rapid thermal oxidation (RTO) at 850 °C for 30 s for **HT-NW** and **HT-GAA** samples. On the other hand, a 3-nm thick tunneling oxide was grown by Inductively Coupled Plasma Chemical Vapor Deposition (ICP-CVD) at 425 °C for **LT-NW** and **LT-GAA** samples. After that, stacked trapping layer with a 3-nm thick Si_3N_4 deposited by ICP-CVD and a 7-nm thick HfO_2 deposited by an atomic layer deposition (ALD) system was formed on all samples. An 18-nm thick Al_2O_3 blocking layer was then deposited by ALD. A 100-nm thick TiN metal gate was deposited by a physical vapor deposition (PVD) system. After gate region was defined and transferred, standard passivation and metallization processes were performed, followed by a sintering at 400 °C for 30 min to complete the fabrication of devices.

3. Results and Discussion

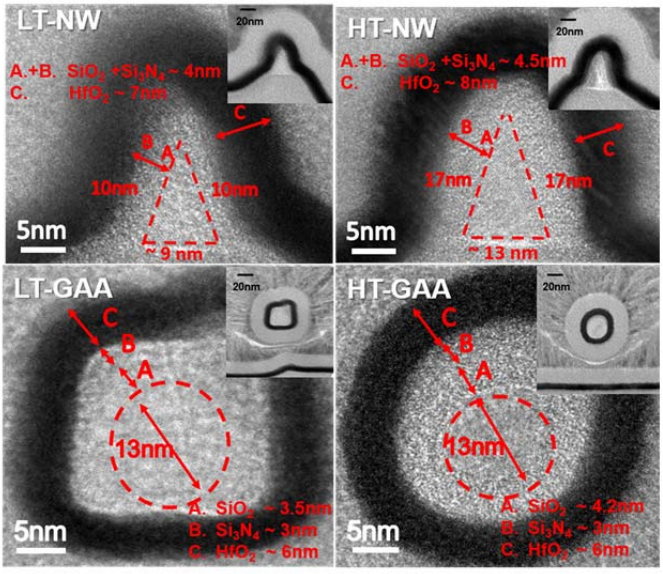

Fig. 1 Cross-section TEM image of GAA and Ω-gate NW channel in CT flash devices.

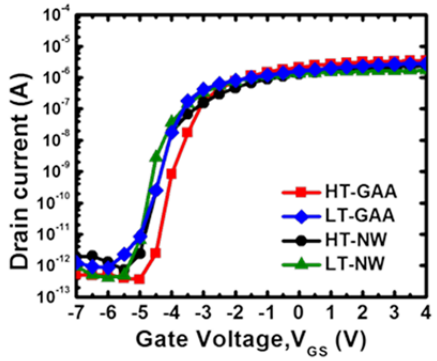

Fig.2 Transfer characteristics of all devices.

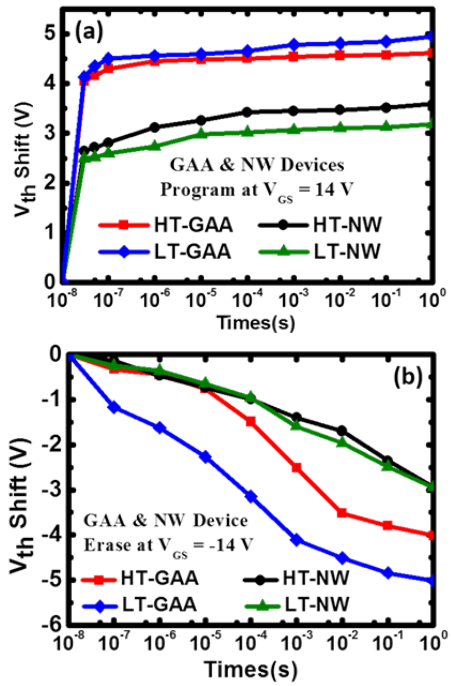

Fig. 3. (a) Programming speed and (b) erasing speed of all devices.

Fig.1 shows transmission electron microscopy images of LT-NW, HT-NW, LT-GAA and HT-GAA devices. Thicknesses of SiO_2 tunneling and Si_3N_4 trapping layers at the channel bottom of LT-GAA device are smaller than those of others due to worse coverage of dielectrics formed by ICP-CVD. Fig. 2 shows drain current (I_{DS}) versus gate voltages (V_{GS}) curves at drain voltage (V_{DS}) = 0.5 V of all samples in this work. The I_{on}/I_{off} ratio is larger than 10^6.

Fig. 3(a) shows the programming speeds of LT-NW, HT-NW, LT-GAA and HT-GAA devices at V_{GS} of 14 V. Both GAA devices show much faster programming speed and larger memory window than Ω-gate NW ones due to higher electric field and more surrounded trapping dielectrics. Fig. 3(b) shows erasing speeds of all devices at V_{GS} of -14V. The erasing speeds of GAA devices are faster than those of Ω-gate NW ones. LT-GAA device shows the fastest erasing speed among all. This may be attributed to less coverage of SiO_2 and Si_3N_4 at the bottom of channel for GAA samples formed by ICP-CVD. The trapped electrons in LT-GAA devices are easier to detrap from trapping layers

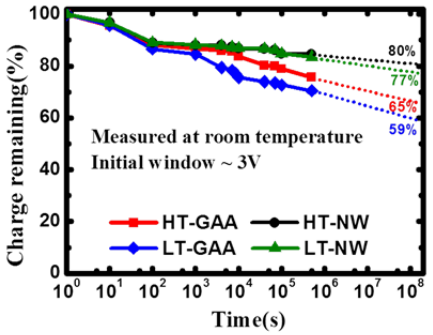

Fig. 4. Retention characteristics of all devices

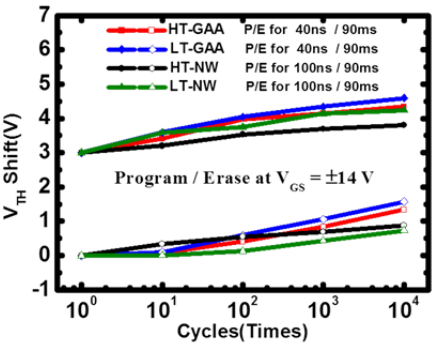

Fig. 5 Endurance characteristics of all devices.

through the bottom of channel due to thinner SiO_2 and Si_3N_4. The erasing speeds of GAA devices become faster after ~10^{-5} s, suggesting that most trapped charges after programming are located in HfO_2 due to thinner LT formed Si_3N_4. The erasing speed in the beginning of HT-GAA device is not as fast as that of LT-GAA because HT-formed SiO_2 tunneling layer at the bottom of channel is thicker.

Fig. 4(a) shows retention characteristics of all samples in this work. All devices were programmed for a memory window of 3 V and tested at room temperature. The retention performance of LT-GAA device is the worst among all due to less coverage of SiO_2 and Si_3N_4 at the bottom of channel. The retention characteristics of GAA devices are worse than those of Ω-gate NW ones. The endurance characteristics of all samples in this work are shown in Fig. 5. All devices keep a memory window of ~3 V even after 10^4 P/E cycles.

4. Conclusions

Effects of LT formed SiO_2 tunneling and Si_3N_4/HfO_2 stacked trapping layers on CT flash devices with GAA and Ω-NW configurations were investigated. Faster operation speed and larger memory window are achieved by GAA configuration. The less coverage of LT deposited dielectrics at the bottom of channel should be resolved to improve retention characteristics of GAA CT flash devices.

References

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