

Investigation of bias polarity dependence on set operation in phase change memory using GeCu₂Te₃

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Abstract

We measured the impact of the thermoelectric effect, especially the Peltier effect, on the operation of the phase change memory (PCM) where the contact resistance between phase change material and electrode is dominant in the total resistance. A PCM device having a pillar structure with a diameter of 500 nm was fabricated using GeCu₂Te₃ (GCT) material. As PCM devices become nano-size, research on contact resistance and various related effect will become more important.

1. Introduction

Phase change memory (PCM), one of the next generation memories, is the spotlighted non-volatile memory because of fast speed, high scalability and multi-level property [1-3]. In nanoscale PCM, the comprehensive effect of interfacial property and thermoelectric heating becomes more important [4-6]. S. Shindo *et al* researched the contact resistivity of Ge₂Sb₂Te₅ (GST) and GeCu₂Te₃ (GCT) by phase-change state [4]. GST itself has the larger resistance ratio of crystallization and amorphous than GCT. However, in a nano-size device, the total resistance is dominated by the contact resistance and the contact resistance ratio is larger in the case of GCT. This implies that GCT has better memory window than GST. Kyle L. Grosse *et al* measured the contact resistivity of the PCM and observed the influence of Peltier and crowding effects [5]. In GST, Joule heating is a factor of temperature generation for operation, but Peltier heating also affect.

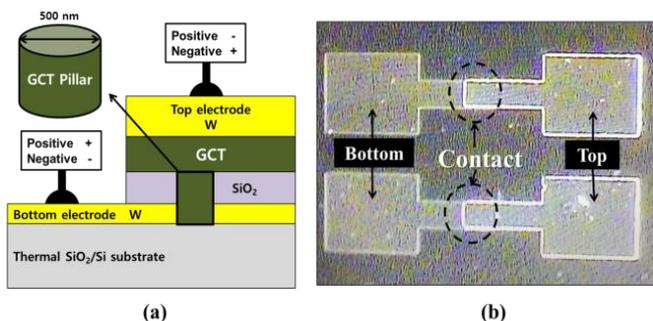


Fig. 1 (a) the vertical schematic and (b) top view of the PCM device.

In this study, we fabricated and estimated the PCM devices using GCT. As a result, we confirmed the effect of contact characteristic on the PCM operation.

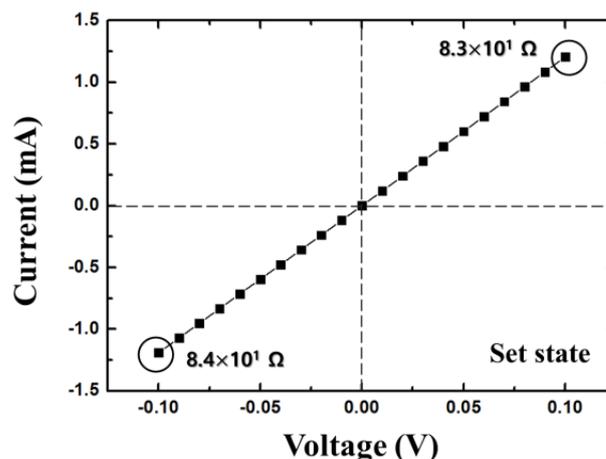


Fig. 2 Read operation in Set state.

2. General Instructions

Fabrication device

Figure 1 shows the cross section diagram (a) and top view (b) of the PCM device using GCT as a phase-change material and tungsten (W) as an electrode. The fabrication process of the device is as follows. First of all, the bottom electrode (50 nm) patterned by lithography and oxidation (100 nm) deposited on Si/SiO₂ substrate. Next the contact hole (diameter: 500 nm) is formed by FIB. Then, GCT (300 nm) is sputtered and the patterned top electrode (200 nm) is finally deposited. As a result, PCM device with a cylindrical structure, in which the diameter of pillar and thickness of bottom electrode determine the contact area, is obtained.

Read and Set operation

Figure 2 and 3 are the read operation of each of the set state (crystalline GCT) and reset state (amorphous GCT) in the fabricated device. Here, the read bias is from -0.1 V to +0.1 V. As shown in the set state of Fig. 2, 8.4 × 10¹ Ω is measured at -0.1 V and 8.3 × 10¹ Ω at +0.1 V. The equivalent resistance regardless of the bias direction means the ohmic contact between GCT and electrode. In contrast, the

schottky contact is verified as $4.3 \times 10^4 \Omega$ at -0.1 V and $3.5 \times 10^5 \Omega$ at $+0.1$ V in reset state. As the phase change occurs between crystalline and amorphous state, the band gap also is changed by the valance band shift [7]. Consequently, the contact barrier between phase change material and electrode causes the alteration of contact mechanism. Especially, the schottky contact affects not only the read resistance but also the set operation by the bias polarity on account of Peltier effect. Ideal Peltier effect equation of p-type semiconductor is as follows.

$$Q' = \pm \pi I \quad (1)$$

$$\pi = \frac{1}{e} [(E_{Fp} - E_V) + \frac{3}{2} kT] \quad (2)$$

Where Q' is the heat generation at contact region, π is the Peltier coefficient, I is the electric current, E_{Fp} is the fermi-level of the p-type semiconductor, E_V is the valence band level, k is the Boltzmann's constant and T is the absolute temperature. The sign of the Peltier coefficient is determined by the direction of the bias, also heating and cooling are generated respectively at the positive and negative sign.

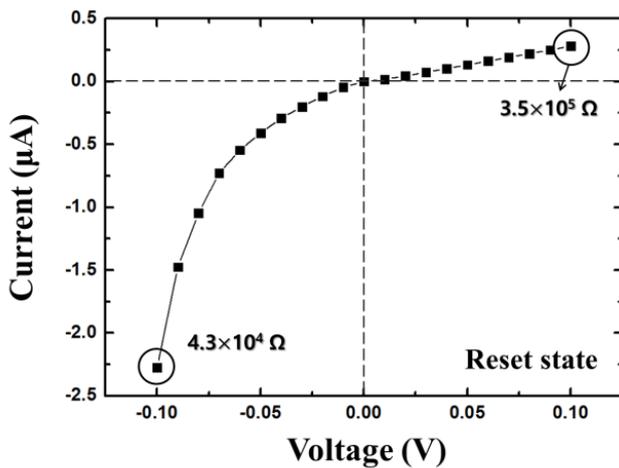


Fig. 3 Read operation in reset state

Figure 4 indicates the set operation by bias direction of $0 \sim \pm 1.5$ V with the step of 0.1 V. The reset resistance began to drop at 1.8 V in the positive direction. In negative direction, however, the resistance decreased at 1.4 V. This is because the Peltier coefficient has a positive value and Peltier heating acts in negative direction. But Peltier cooling occurs in negative direction. So, more voltage is needed for the set operation. This Peltier effect reduced the set current by about 25 % in the negative direction relative to the positive direction.

3. Conclusions

We confirmed the reliance of bias polarity on the set operation in PCM. The PCM device using GCT was fabricated and the contact mechanism according to the phase

state was checked through the read operation. In particular, the Schottky contact in the reset state caused the change in set current due to the Peltier effect. This can reduce the set current in negative bias by about 25 % compared with the positive bias.

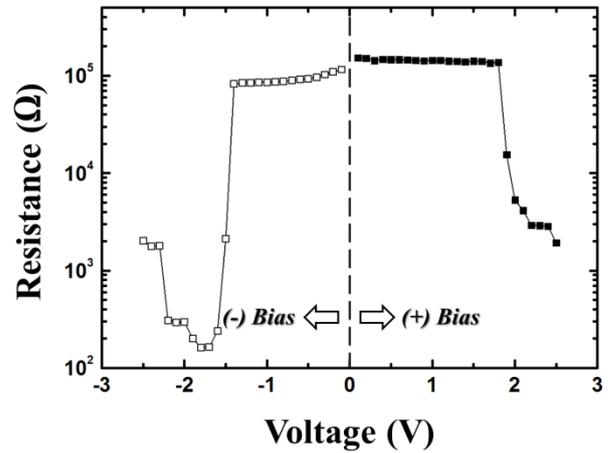


Fig. 4 Set operation by bias direction.

Acknowledgements

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References

- [1] Burr, G. W. et al., *Journal of Vacuum Science & Technology B.* **28** (2010) 223-262.
- [2] Kim, E. H., Kang, N. S., Yang, H. J., Sutou, Y. and Song, Y. H., *Jpn. J. Appl. Phys.* **54** (2015) 094302.
- [3] Bez, R., 2009 IEEE International Electron Devices Meeting (2009) 1-4.
- [4] S. Shindo, Y. Sutou, J. Koike, Y. Saito and Y. H. Song, *Material Science in Semiconductor Processing* **47** (2016) 1-6.
- [5] Kyle L. Grosse et al., *APPLIED PHYSICS LETTERS* **102** (2013) 193503.
- [6] J.H. Lee, M. Asheghi and K. E Goodson, *Nanotechnology* **23** (2012) 205201.
- [7] K. Kobayashi and M. Kobata, *JPCOS* (2013) S42.