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Temperature Sensors with Negative and Positive Temperature Coefficients by Using Cascoded Diode-connected Sub-threshold NMOSFETs and PMOSFETs

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Abstract

This paper analyses the feasibility of using cascoded diode-connected metal–oxide–semiconductor field-effect transistors (MOSFETs) operating in sub-threshold region to implement high-sensitivity and high-linearity temperature sensors with negative and positive temperature coefficients. The cascoded structure is biased by a mirrored current coming from a current reference. The influence of bias current and body effect in MOSFET on linearity and sensitivity is studied. The temperature characteristics of the drain voltages of the cascoded structures using N-type and P-type MOSFETs, respectively, are studied. The measurement results exhibit the sensitivities of -4.38 and 5.42 mV/°C with linearity of 99.9970% and 99.9958%, respectively, over a temperature range from 0 to 100 °C. Temperature dependence of the drain voltage of the cascoded diode-connected sub-threshold MOSFET, which is closer to the transistor of current mirror, exhibits much higher sensitivity and good linearity.

1. Introduction

Bipolar junction transistor (BJT) based temperature sensors have been widely studied [1]. Diode-connected metal–oxide–semiconductor field-effect-transistors (MOSFETs) operating in sub-threshold region have similar current-voltage characteristics to those of BJTs. Recently, the temperature sensors based on diode-connected MOSFETs have been presented [2-4]. The gate-source voltage V_{GS} of the diode-connected sub-threshold MOSFET with a constant bias current exhibits linear temperature dependence. But there still exists non-negligible nonlinearity over a large temperature range. A cascoded configuration consisting of three diode-connected NMOSFETs has been used to implement temperature sensors which have large sensitivity and high linearity owing to the body effect in MOSFET [4]. In this paper, the temperature characteristics of the cascoded structures using N-type and P-type MOSFETs are studied. The temperature sensor has been implemented by TSMC 0.18um processes. The supply voltage is 1.8V. The temperature within the constant temperature cabinet, in which temperature characteristics of sensors are measured, is calibrated by commercial platinum probes.

2. Sensing Design

Figs. 1(a) and 1(b) show the circuit schematics of cascoded diode-connected sub-threshold PMOSFETs and NMOSFETs with a current bias from a current reference, respectively. The current reference for PMOSFETs is a bandgap current reference. The current reference for NMOSFETs is a current-adjustable circuit to study the influence of the bias current on the sensitivity and linearity of the temperature characteristics of output drain voltages.

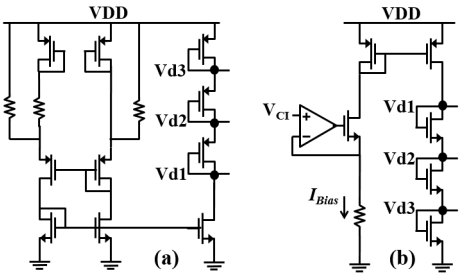

Fig. 1 Circuit schematics of cascoded diode-connected sub-threshold (a) PMOSFETs and (b) NMOSFETs with a current bias from a current reference

For a diode-connected NMOSFET with a constant bias current, the gate-source voltage V_{GS} is equal to the drain-source voltage V_{DS} and the sub-threshold drain current I_D of the MOSFET is an exponential function of the V_{GS} and the V_{DS}. The I_D can be expressed by

$$I_D = \frac{W}{L}\mu C_{ox}(\eta - 1)V_T^2 \exp(\frac{V_{GS}-V_{TH}}{\eta V_T})[1-\exp(-\frac{V_{DS}}{V_T})] \quad (1)$$

where μ is the mobility of carriers, C_{ox} is the gate-oxide capacitance, $V_T = k_B T/q$, k_B is the Boltzmann constant, V_{TH} is the threshold voltage of a MOSFET, and η is the sub-threshold slope factor. For $V_{DS} \geq 3V_T$, the current I_D is almost independent of V_{DS} and hence V_{GS} can be expressed by

$$V_{GS} = V_{TH} + \eta V_T \ln(\frac{I_D}{\mu C_{ox}\frac{W}{L}(\eta-1)V_T^2}) \quad (2)$$

The V_{GS} can be obtained through detailed derivation and then is expressed by [2, 4]

$$V_{GS} = V_{TH0} + \beta(T-T_0) + \gamma\sqrt{2\phi_F}\, f(\frac{V_{SB}}{2\phi_F}) + [1 + \frac{1}{C_{ox}}\sqrt{\frac{\varepsilon_S \varepsilon_0 q N_A}{2[2\phi_F + V_{SB}]}}]\times$$
$$[\ln(\frac{I_D}{\mu_0 \frac{W}{L}\sqrt{\frac{\varepsilon_S \varepsilon_0 q N_A}{2[2\phi_F + V_{SB}]}}V_{T0}^2}) + (\alpha+2)\ln\left(\frac{T_0}{T}\right)]\frac{k}{q}T \quad (3)$$

In eq. (3), the first term is a constant and the second term

has linear negative dependence on temperature because β is negative. The third term is related to the body effect and this term introduces a negative temperature coefficient in the $V_{GS}(T)$ if the V_{SB} decreases with the increase of temperature. The last term shows that the sensitivity can be enhanced by using smaller bias current and larger device size. The bias current with more positive TC results in smaller sensitivity of gate voltages because the fourth term will introduce in a corresponding positive temperature dependence.

In summary, the magnitude $|V_{DS}(T)|$ of the voltage drop between drain and source of a sub-threshold MOSFET decreases with increasing temperature. Thus the temperature coefficient (TC) of the output drain voltages of the cascoded sub-threshold NMOSFETs and PMOSFETs will have a negative and a positive value, respectively. The smaller bias current and decreasing body effect with increasing temperature can result in a larger voltage variation with temperature. Moreover, the TC of the drain voltage (i.e., Vd1) of the transistor closer to the transistor of the current mirror is enhanced because its $|V_{SB}|$ decreases more with increasing temperature and then the reduction of body effect makes the voltage drop between gate (i.e., drain) and source much smaller.

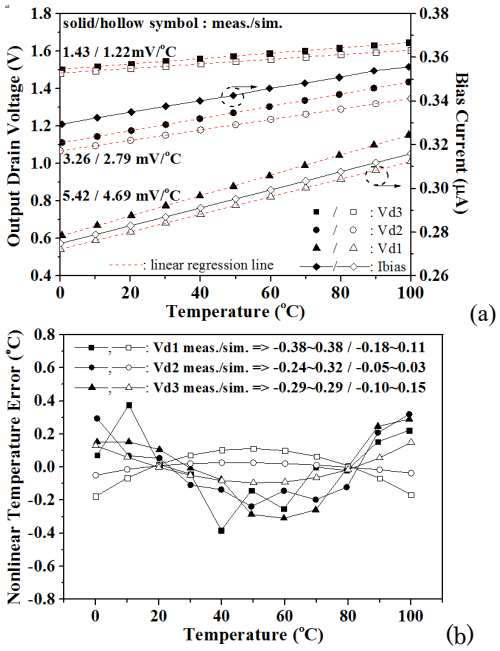

Fig. 2 Simulated and measured (a) output drain voltages against temperature, its linear regression line and (b)nonlinear temperature error.

Fig. 2 shows simulated and measured temperature characteristics of output drain voltages of the circuit in Fig. 1(a). Its linear regression line and nonlinear temperature error are also shown. The sensitivities and temperature error ranges are also listed in the figures. Measured and simulated bias currents is proportional-to-absolute-temperature (PTAT). The simulated sensitivity is smaller probably because its bias current has more positive temperature dependence. The Vd1 is actually enhanced to a much larger sensitivity due to the existence of body effect. The nonlinear temperature errors are +/-0.4 °C over a temperature range from 0 to 100 °C.

Fig. 3 shows measured temperature characteristics of output drain voltages of the circuit in Fig. 1(b). Its linear regression line and nonlinear temperature error are also shown. The sensitivities and temperature error ranges are also listed in the figures. The bias currents of around 0.6 and 2.6 μA, which can be adjusted by V_{CI}, are used. The smaller current results in more negative sensitivity. The temperature characteristics of drain voltages exhibit negative TCs.

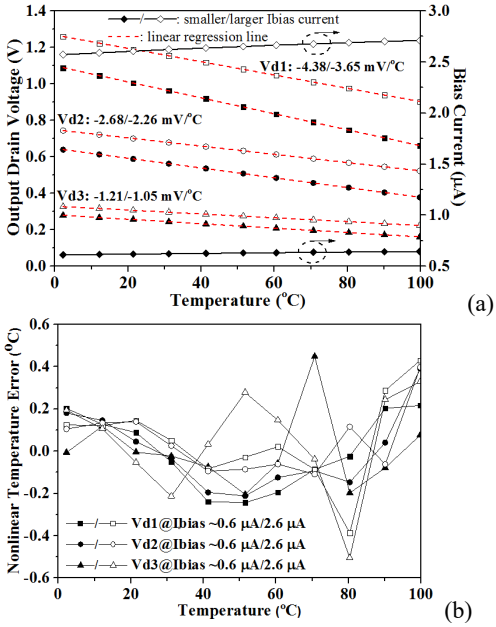

Fig. 3 Measured (a) output drain voltages against temperature, its linear regression line and (b) nonlinear temperature error. The circuit is shown in Fig. 1(b)

3. Conclusions

Experimental results show that the existence of body effect in MOSFET can enhance sensitivities of temperature characteristics of the drain voltages of the cascoded MOSFETs and linearity is good. The larger sensitivity can be obtained by using a smaller bias current. Therefore, temperature sensor with low power consumption can be implemented. The drain voltages of the cascoded diode-connected sub-threshold PMOSFETs and NMOSFETs exhibit positive and negative TCs. respectively.

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