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# A Cyclic Switched-Capacitor Step-Down DC-DC Regulator with Enhanced Output Current

Wei-Liang Wang, Hongchin Lin and Chang-Lin Yu

Dept. of Electrical Engineering, National Chung Hsing University, Taichung, Taiwan
Phone: +886-4-2284-0688 ext. 250 E-mail: hclin@ nchu.edu.tw

**Abstract**

**A 3-phase cyclic switching capacitor (SC) step-down DC-DC regulator is proposed and was implemented using 0.25μm CMOS technology. The dual output voltages of 1.5V and 3.0V using conversion ratios (CRs) of 1/3 and 2/3 are obtained with 5V input voltage and 1nF on-chip flying capacitors ($C_f$). The measured maximum total output current is 8.9 mA at frequency ($f$) of 20.8 MHz with power efficiency (η) of 70%. The normalized output current ($I_{norm}$) is 0.428 A/(F·Hz).**

## 1. Introduction

Owing to the advance of the CMOS technologies and the trends of low power consumption, different circuits may work at different low supply voltages, so a DC-DC inductor-based or capacitor-based step-down regulator is required. The former can provide high output currents with high efficiency (η) [1] but needs external bulky inductors. The later named switched capacitor (SC) regulator can be integrated in one chip with less output current and is appropriate for portable devices. The ideal η of SC regulator is determined by the conversion ratio (CR), the input voltage and the output voltage. The higher η is, the less output current is. Thus, the trade-off is inevitable. Here, a cyclic SC topology is proposed for CR = 1/3 to enhance output current without ideal η degradation compared to that of the conventional approach [2]. Besides, CR of 2/3 can be generated at the same time. The dual output voltages like inductor-based converters [1] are also demonstrated by the cyclic SC step-down regulators.

The popular regulation methods of SC regulators are pulse frequency modulation (PFM) [3, 4] and voltage controlled oscillation (VCO) [5, 6]. The frequencies are adjusted by the control loop, so the stability has to be carefully analyzed. Furthermore, for applications of portable wireless communication devices, the variable frequencies may cause problems of electromagnetic interference (EMI). To avoid EMI, the low dropout regulators (LDOs) with the constant frequency based cyclic SC network were adopted.

## 2. Operation of Cyclic Switched Capacitors

The conventional SC operation of CR = 1/3 with charging and discharging 4 identical capacitors at the same time [2] is shown in Fig. 1. The switches with N and P in Fig. 1 (b) indicate NMOS and PMOS transistors, respectively. The number of switches are 7×2=14 owing to the two phases. If the current factor ($I_f$) is defined as the ideal output current divided by $C_f \times V_{DD} \times f$, $I_f = 3C \cdot \Delta V \cdot 2f/(4C \cdot V_{DD} \cdot f) = 3/40$, where $\Delta V = 0.5V/2 = 0.25V$.

The proposed cyclic SC operation of CRs = 1/3 and 2/3 using 3 phases is shown in Fig. 2. The number of switches are 4×3=12 if out2 is not needed and one NMOS transistor can be shared in two phases, and the current factor $I_f = 1.5C \cdot \Delta V \cdot 3f/(3C \cdot V_{DD} \cdot f) = 1/10$, where $\Delta V = 0.5V/1.5 = 1/3V$. Therefore, the number of switches is less and the current factor is higher than those of the conventional topology.

## 3. Architecture and Circuits

The architecture is illustrated in Fig. 3. The SC network is followed by two LDOs to produce Vout1 = 1.5V and Vout2 = 3.0V. The block diagram of the SC network consisting of 3 circuit blocks is shown in Fig. 4(a). Each block requires 2 out of the 3 non-overlapping clocks sketched in Fig. 4(b). The detailed circuit of the block of C1_switch is shown in Fig. 4(c). The other 2 blocks are identical except the clocks using different clock phases. The links between the blocks are nodes 3_2, 2_1, 1_3.

## 4. Experimental Results

The proposed 5V converting to 1.5V and 3.0V DC-DC regulator was implemented on area of 1.032mm$^2$ by 0.25μm CMOS technology. The die microphotograph is shown in Fig. 5. In Fig. 6, the measured waveforms of the two outputs (Vout1 and Vout2) show good transient characteristics when Iout2 = 3.9 mA and Iout1 is switched between 0.1mA and 5 mA. The simulated and measured load regulation and η of the two outputs are quite close as shown in Fig. 7.

## 5. Comparison

Table I compares performance of the recent published literature. Since the output current, output voltage, input voltage, $C_f$, CR, frequency, and technology are different. The normalized output current given below indicates the output current of the proposed SC topology per unit capacitance is the highest.

$$\mathrm{I_{norm}} = \frac{\mathrm{I_{load(max)}}}{C_f \times \mathrm{Frequency}}$$

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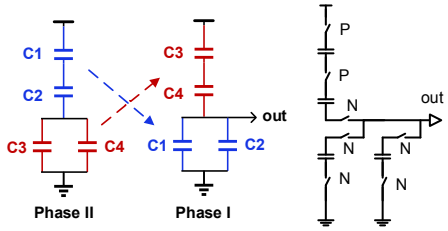
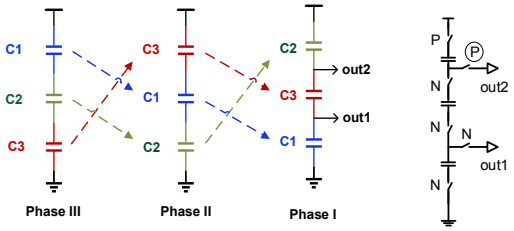


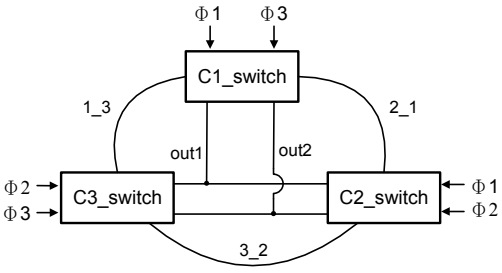

(a) Switching operation (b) Switches

Fig. 1 The conventional SC with CR=1/3

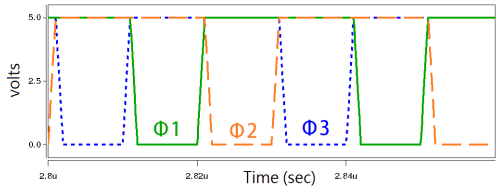



(a) Switching operation (b) Switches

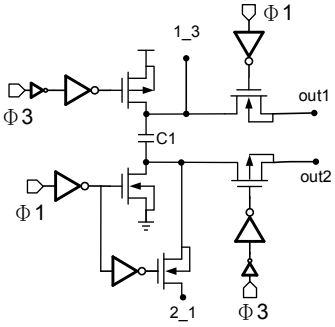
Fig. 2 The proposed cyclic SC with CRs =1/3 and 2/3




(a) The block diagram




(b) The 3-phase non-overlapping clock scheme




(c) The circuit of block C1_switch in (a)

Fig. 4 The circuit of switched capacitor network

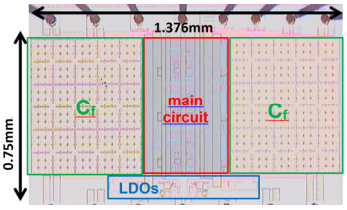



Fig. 5 The die microphotograph

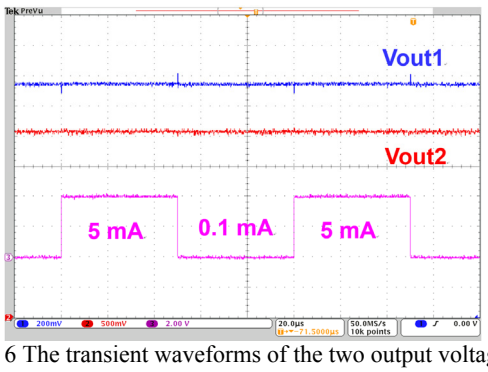



Fig. 6 The transient waveforms of the two output voltages

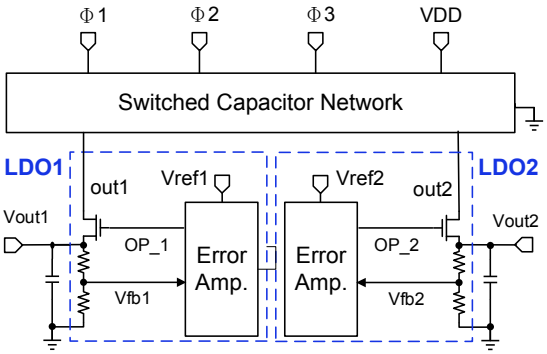
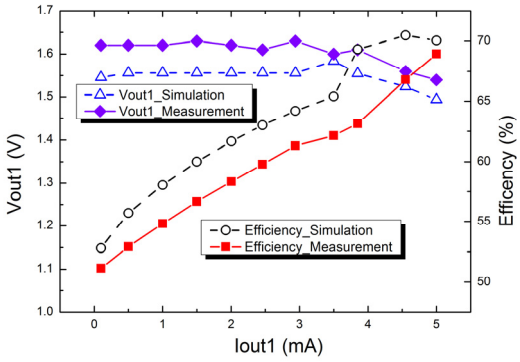
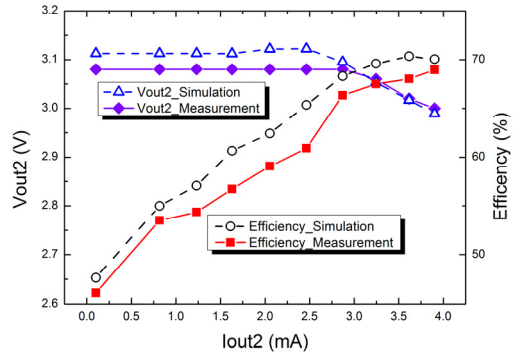



Fig. 3 The architecture of the proposed cyclic SC regulator




(a) Vout1 and η vs. Iout1 when Iout2 = 3.9 mA




(b) Vout2 and η vs. Iout2 when Iout1 = 5 mA

Fig. 7 Output voltages and efficiency vs. output currents

Table I Comparison of on-chip step-sown DC-DC regulators (Ref. [2] is based on the simulation results)

| | 13 TVLSI [2] (sim.) | 14 JSSC [3] | 16 TCAS [4] | 12 ISSCC [5] | 17 JSSC [6] | This Work |
|---|---|---|---|---|---|---|
| Technology | 40nm | 250nm | 65nm | 90nm | 65nm | 250nm |
| Regulation | Hysteretic | PFM | PFM | VCO | VCO | LDO |
| $V_{DD}$ (V) | 1.1 | 2.5 | 0.6~1.2 | 1.2~2 | 1.6~2.2 | 5 |
| $V_{out}$ (V) | 0.18-0.6 | 0.2-1.6 | 0.6, 0.8, 1 | 0.7V | 0.6~1.2 | 1.5 & 3 |
| $C_{fly}$ | 742pF | 2.8nF | 675pF | 1.148nF | 4.8nF | 1nF |
| Frequency | 26MHz | 9MHz | 13MHz | 50MHz | 33MHz | 20.8MHz |
| Peak η | 90.35%@ Vdd=0.53V | 85% | 80%@ Vout=1V | 81% | 80% | 70% |
| Ideal η | 96.4% | NA | 83.33% | 87.5% | 86.8% | 90% |
| $I_{load(max)}$ (mA) | 1 | 1.86 | 0.8 | 8 | 50 | 5+3.9 |
| **$I_{norm}$ (A/(F·Hz))** | **0.0518** | **0.074** | **0.0911** | **0.139** | **0.315** | **0.428** |
| Area ($mm^2$) | 0.074 | 4.33 | 0.493 | 0.25 | 0.84 | 1.032 |
| CR | 1/4, 1/3, 1/2, 2/3 | 1/3, 1/2, 2/3 | 2/3, 3/4, 1 | 1/2, 2/3 | 1/2, 2/3, 3/4 | 1/3, 2/3 |