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A 0.45-to-1.8 GHz Fully Synthesized Injection Locked Bang-Bang PLL with OFDAC to Enhance DCO resolution

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***Abstract*—This paper presents a fully synthesized injection locked bang-bang phased-locked loop (SILBBPLL) with ultra-fine DCO resolution. A novel ultra-fine frequency tuning block is proposed to improve the DCO resolution. A standard cell based output feedback DAC (OFDAC) is adopted for the ultra-fine frequency tuning. The proposed SILBBPLL is described in hardware language and automatically placed & routed by using standard digital circuit design flow. It is implemented in 65 nm CMOS with an active area of 0.008 mm^2. The measured results show that power consumption of the SILBBPLL operating at 1.5 GHz is 1.8 mW @0.8V. The integrated root-mean-square (RMS) jitter is equal to 0.91 ps. The SILBBPLL achieves a figure-of-merit (FOM$_a$) of -259.1 dB.**

1. Introduction

Synthesized PLLs [1]–[5] have advantages of significantly short design period, enhanced portability and scalability between different process technologies. A digital control oscillator (DCO) with fine frequency tuning resolution is the most critical block for a fully synthesized PLL. The previous fully synthesizable PLLs based on standard cells have a limited DCO frequency tuning resolution, which result in poor jitter performance [2]. In [3]-[5], although the PLLs were designed and automatically placed & routed (APR), a costly custom DCO was manually layout designed firstly then synthesized in PLLs. A custom DCO block still needs a heavy layout effort and the advantages of the synthesized PLL were degraded.

This paper proposes a fully synthesized injection locked bang-bang phased-locked loop (SILBBPLL) with ultra-fine DCO resolution. A novel ultra-fine frequency tuning block is proposed to improve the DCO resolution. A standard cell based output feedback DAC (OFDAC) is adopted for the ultra-fine frequency tuning. The pulse injection-locked technique is adopted to reduce the phase noise. With the proposed techniques, this paper can solve the problems of limited resolution [2], poor phase noise and heavily manual layout [3]-[5] of the traditional synthesized PLLs. Design period is greatly reduced and the portability and scalability of the PLL can be guaranteed.

2. Architecture of the SILBBPLL

Fig.1 shows the architecture of the proposed SILBBPLL. It consists of a DCO, three OFDACs, a binary to thermometer (B-T) converter, injection-locking circuits and two loops (PLL1 and PLL2). With the injection locking, the phase noise of the SILBBPLL can be greatly reduced. The SILBBPLL is APR by the standard digital design flow. Therefore, the design period is greatly reduced.

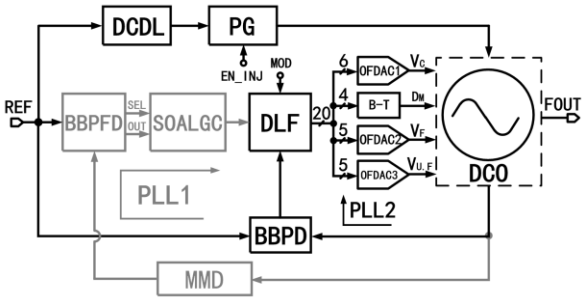


Fig. 1. Block diagram of the synthesized SILBBPLL.

3. Implementation and fabrication

DCO overall structure

The overall DCO architecture with frequency tuning blocks is presented in Fig. 2. The DCO is designed as 4 stage differential structure. A 20-bit frequency control words scheme is used for the frequency tuning of the DCO, in which 6 bits are used for coarse tuning, 4 bits are used for medium tuning, 5 bits are set for fine tuning and 5 bits are set for ultra-fine tuning. An NMOS transistor is added in the standard cell library as the injector of the DCO. OFDAC1 is used for coarse tuning of the DCO. OFDAC2 and OFDAC3 are adopted for the fine tuning and ultra-fine tuning of the DCO, respectively.

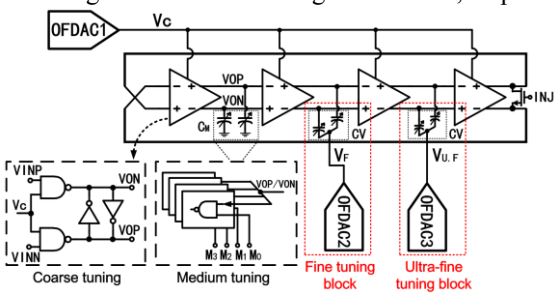


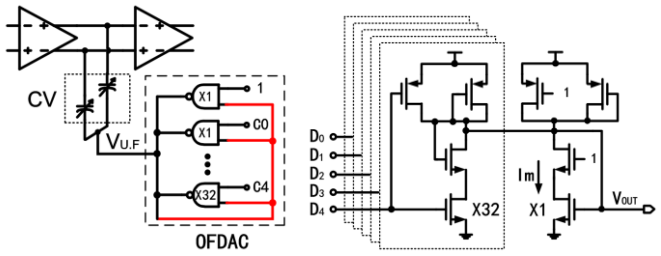
Fig. 2. The overall DCO architecture with frequency tuning blocks.

Ultra-fine frequency tuning block

In order to improve the resolution of the standard cell based DCO, a custom varactor (CV) is added into the standard

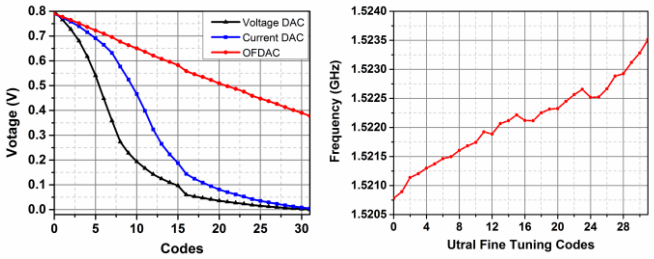
cell library for ultra-fine tuning of DCO. So the whole SILBBPLL can be fully synthesized with ultra-fine DCO resolution. A 5-bit OFDAC with high converted linearity is exploited to provide linear tuning voltage for the CV. The ultra-fine frequency tuning block is shown in Fig. 3 (a) and the detailed schematic of OFDAC is presented in Fig. 3 (b).

The OFDAC is built with NAND gates in the standard cell library [4]. Digital control word D_N is used to control the on/off of the inverter or NAND gate. When D_N becomes larger, the output voltage becomes smaller. Fig. 4 (a) shows the simulated converted characteristic of the OFDAC. Compared with the traditional inverter based voltage DAC and the current DAC in [1], the OFDAC has a merit of high linearity. Therefore, the OFDAC can be used as a voltage tuning block for the custom varactor, which leads to a high linearity of the proposed ultra-fine tuning block. Fig. 4 (b) presents the post layout tuning characteristic of the ultra-fine tuning block. With the help of proposed ultra-fine tuning block, DCO frequency ranges from 1.5208 GHz to 1.5235 GHz with promising linearity and an average resolution of 91 kHz/LSB.



(a) (b)

Fig. 3. (a) Ultra-fine frequency tuning block, (b) Schematic of OFDAC.



(a) (b)

Fig. 4. (a) OFDAC converted characteristic, (b) tuning characterristic of the ultra-fine tuning block.

4. Measurement results

The SILBBPLL is implemented using standard digital design flow in a 65 nm CMOS process. Die photograph is shown in Fig. 5. It occupies an active core area of 0.008 mm^2. Power consumption is 1.8 mW at a frequency of 1.5 GHz, with a source supply of 0.8 V.

Fig. 6 shows the measured phase noise and frequency spectrum of 1.5 GHz without and with injection locking respectively. Reference clock is 150 MHz. RMS jitter with injection locking integrated from 1 kHz to 30 MHz is 0.91 ps. With injection locking, the reference spur level at 150 MHz is -51.6 dBc. Table I summarize the performance of this work and the recently published synthesized PLLs.

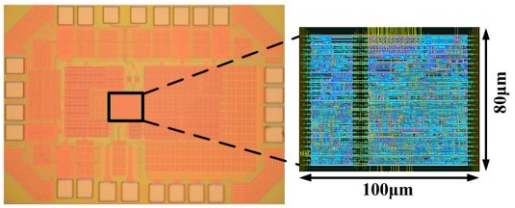
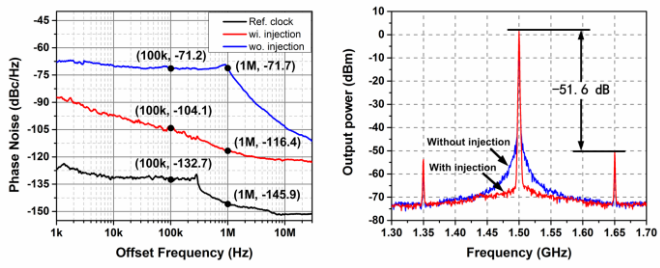


Fig. 5. Die microphotograph.



(a) (b)

Fig. 6. (a)Measured phase noise,(b) Frequency spectrums at 1.5 GHz with and without injection, respectively.

Table I Performance summary and comparison

	This work	JSSC2016 [3]	JSSC2015 [1]	ESSCIRC 2016 [4]
Technology	**65nm**	65nm	65nm	65nm
Freq. [GHz]	**0.45 – 1.8**	2	0.39—1.41	2.8—3.2
Ref.[MHz]	**150**	64	40-350	150
Power [mW]	**1.8@1.5G**	10.8@2G	0.78@0.9G	4.6@3G
Area [mm^2]	**0.008**	0.047	0.0066	0.12
RMS jitter [ps] (range)	**0.91 [1k~30M]**	3.15 [10k~100M]	1.7 [10k~40M]	0.142 [10k~40M]
Ref. spur [dBc]	**-51.6**	—	-42	-47
FOM_a [dB][a]	**-259.3**	-233	-258.3	-259.5
Fully Synthesized	**Yes**	No	Yes	No

[a] $FOM_a = 20\log(\sigma_t/1s) + 10\ \log(P/1mW) + 10\log(A/1mm^2)$.

5. Conclusions

This paper presented a fully synthesized injection locked bang-bang phased-locked loop (SILBBPLL) with ultra-fine DCO resolution. With the proposed techniques, the SILBBPLL achieved a FOM_a of -259.3 dB.

Acknowledgment

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