AlGaN/GaN Schottky Gate Fin-HEMT Fabricated on 8-inch Silicon (111) Substrate with Thin Buffer Layer

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Abstract
In this letter, we demonstrate the AlGaN/GaN Fin-HEMT on 8-inch Si (111) substrate with thin AlGaN buffer which is about 3 μm. This Fin-HEMT is characterized by the Schottky gate without any insulating dielectric. This Schottky gate creates the depletion region on both sidewalls of the fin channel can further deplete the carrier. This sidewall assistant makes the device turns off earlier than planar device which is confirmed by the positive shift of the threshold voltage ($V_{TH}$). The minimum fin width is characterized by 100 nm and the corresponding $V_{TH}$ is -0.5 V which has 3.05 V shift from the planar device.

1. Introduction
Owing to the superior material properties such as high breakdown field, low ON-resistance ($R_{ON}$), and high thermal stability, GaN-based high-electron-mobility transistors (HEMTs) have huge potential of the applications in power electronics [1-3]. In terms of material properties, AlGaN/GaN heterojunction exhibits 2DEG inherently due to its unique properties of polarization but also results in normally-ON operation. For the normally-ON, i.e., enhancement-mode (E-mode) device, it is more complicated for circuit design and less output efficiency. In this paper, we utilize the fin-shaped channel to modulate the threshold voltage ($V_{TH}$) toward positive value [4,5]. The gate metal in our Fin-HEMT is deposited directly on the AlGaN/GaN fin channel to form the Schottky contact on all sides of fin. It should be noted that the Schottky contact has wider depletion width than the metal-insulator-semiconductor contact. Therefore, once the fin becomes narrow enough, it is possible to fully deplete 2DEG through the sidewall depletion region earlier than the top-gate control. This leads to the positive $V_{TH}$ movement and the switching mechanism is similar to the metal-semiconductor field-effect transistor.

2. Device Fabrication
The epitaxial structure of AlGaN/GaN is grown by MOCVD and starts on 8 inch silicon wafer with a 300 nm AlN nucleation layer, ~3.2 μm graded AlGaN buffer, 2 μm undoped GaN layer, 30 nm undoped Al$_{0.3}$Ga$_{0.7}$N barrier, and 1 nm undoped GaN cap layer. The specific layer structure is shown in Fig. 1 (a). After the material growth, hall measurement is implemented form the center to the edge of wafer with 9 points. The results show that peak and average mobility is 1520 cm$^2$/Vs and 1323 cm$^2$/Vs, respectively which suggest that high uniformity of the epitaxy.

The process flow and schematic diagram of device are shown in Fig. 1 (b) and the device is begun with fin formation. The minimum fin width ($W_{fin}$) here is 100 nm which defined by the electron-beam lithography and is etched by the Cl$_2$/BCl$_3$ mixed plasma. The Ti/Al/Ni/Au deposition and rapid thermal annealing is then applied in sequence to form the S/D Ohmic contact. Finally, gate metal with Ni/Au is deposited to complete the device. It should be noted that gate metal is deposited directly on the fin channel to form the Schottky contact on all sides. Fig. 2 is the SEM image of the device with 100 nm $W_{fin}$. The fin number of 100 nm $W_{fin}$ is 100 and thus we can defined the projective channel width is the production of $W_{fin}$ and fin number.

3. Results and Discussions
The comparison of the transfer characteristics with different $W_{fin}$ is shown in Fig. 3 (a). We can observe that the $V_{TH}$ of the fin device has significant shift toward positive value comparing to planar one. The $V_{TH}$ of device with $W_{fin}$ of 100 nm and gate length ($L_g$) of 2 μm is characterized by -0.7 V and the planar one is -3.75 V with the same $L_g$ and the gate width ($W_g$) is 60 μm. The $V_{TH}$ is defined by the current density of 100 μA/mm normalized by the projective...
channel width. The relation between the $V_{TH}$ and the $W_{fin}$ is also shown in Fig. 3 (b). It can be obtained that while the channel width is in the nano regime, $V_{TH}$ is strongly affected by the $W_{fin}$. This is attributed to the assistant of depletion region on both sidewalls of fin channel. The switching mechanism of Fin-HEMT is shown in Fig. 4. Once the fin is thin enough, the depletion region caused by the sidewall can fully deplete the 2DEG in channel earlier than the top-gate control. That is, the depletion width on each side is larger than the half of $W_{fin}$ in the specific gate bias and thus results in the pinch-off status. Also, by the linear fitting of $V_{TH}$ with different $W_{fin}$ in Fig. 3 (b) the device with $W_{fin}$ less than 35 nm can obtain the E-mode operation through the side-gate control. And device with the $W_{fin}$ larger than 360 nm, it becomes the top-gate control which is just like the planar one.

The output characteristics of device with 2-μm $L_g$ and 150-nm $W_{fin}$ is shown in Fig. 5 (a). The saturation drain current is 73 mA/mm. This relatively low value is attributed to large source/drain resistance ($R_{SD}$) of 35.83 Ω-mm. $R_{SD}$ here is obtained by linear extraction of $R_{ON}$ with different $L_g$ which is shown in Fig. 5 (b). This high $R_{SD}$ is induced by the non-optimized contact resistance and large distance of gate-to-source ($L_{gs}$) and gate-to-drain ($L_{gd}$) (both are 5μm). Therefore, better ON-state performance can be obtained with optimized Ohmic contact and further scaling of the $L_{gs}$ and $L_{gd}$.

Finally, we compare the ON-state performance of device with different $W_{fin}$ which is shown in Fig. 6. Fig. 6 (a) shows the peak transconductance ($g_m$) of device with 2 μm $L_g$. Fin device exhibits higher $g_m$ than the planar one and similar trend of $R_{ON}$ is also obtained in Fig. 6 (b). This is contrary to the conventional Si-based FinFET that thinner fin has larger $R_{ON}$ due to the larger scattering. This is caused by the higher thermal resistance in the larger channel width [6].

4. Conclusions

In this paper, we demonstrate the AlGaN/GaN Fin-HEMT with the Schottky gate contact. This Schottky contact is beneficial to pinch off the channel earlier from the sidewall. The device with minimum $W_{fin}$ of 100 nm exhibits $V_{TH}$ of -0.7 V which has 3.05 V shift form the planar one. The E-mode operation can be achieved with further scaling the $W_{fin}$ down to 35 nm. The device with thinner $W_{fin}$ also shows better ON-state performance which is caused by the lower thermal resistance.

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