PS-6-08

Improved Electrical Stability of Thin-Film Transistors with Co-sputtered Ti-IGZO Channel and $Zr_{0.85}Si_{0.15}O_2$ Gate Dielectric

Hao-Ping Yen [1], Shui-Jinn Wang[1, 2*], Chien-Hsiung Hung [1], Nai-Sheng Wu[1], Ying-Chi Hung[1], Zhi-Kai Zhuang[1], Cheng-Xiu Lin[1], and Chien-Hung Wu[3]

[1] Institute of Microelectronics, Dept. of Electrical Eng., National Cheng Kung Univ., Tainan, Taiwan.
[2]Advanced Optoelectronic Technology Center, National Cheng Kung University, Tainan, Taiwan
[3] Department of Electronics Engineering, Chung Hua University, Hsinchu, Taiwan.
*Phone: +886-6-2763882, E-mail: sjwang@mail.ncku.edu.tw

Abstract:

The use of co-sputtered Titanium doped indium gallium zinc oxide (Ti-IGZO) channel with zirconium silicon oxide ($Zr_{0.85}Si_{0.15}O_2$) as gate dielectrics to improve reliability of thin-film transistors (TFTs) is presented. It is found that oxygen vacancies in Ti-IGZO Channel is decreased after Ti incorporation and stability of the TFTs could be considerably improved. Experimental results reveal that Ti-IGZO channel prepared at a power ratio of IGZO:TiO_2=80 W:25 W with a post deposition annealing (PDA) and with a 9±1-nm-EOT $Zr_{0.85}Si_{0.15}O_2$ layer shows the best device performance with the on/off current ratio, the subthreshold swing, the threshold voltage shift after 1000 sec positive/negative gate-bias stress are of 1.65×10^8, 0.09 V/dec, and 0.157 V/−0.093 V, respectively.

1. Introduction

Highly stable TFT devices are necessary for applications of active-matrix flat-panel display applications (AMFPDs) [1]. Indium gallium zinc oxide (IGZO) has been the main stream of channel material for TFT-related industries, because α-IGZO has a relatively much higher electron mobility for having spherical symmetry S orbits resulting from In incorporation. Nevertheless, because of the existence of dense interstitial Zn atoms and oxygen vacancies originating from frangible In-O bonds, α-IGZO TFTs are liable to incur reliability issue caused by charge trapping via defect states within or at the surface of the α-IGZO channel. Through a suitable incorporation of oxidizable Titanium (Ti) in α-IGZO to enlarge bandgap and lower the donor energy level, benefits including suppression in trap state density and leakage current as well as device reliability enhancement has been demonstrated [1]. Recently, α-IGZO TFTs with a stacked IGZO/TiO_2 channel was reported and effectiveness of the TiO_2 layer on suppressing interface trap density was clarified [2].

In this study, a simple co-sputtering process with IGZO and TiO_2 targets at room temperature (RT) is proposed to incorporate Ti with α-IGZO. Through adjusting the power of TiO_2 target during sputtering deposition, effects of Ti content on channel material and device performance and reliability are studied. The optimum RF power ratio and post deposition annealing (PDA) to realize a suitable Ti content in α-IGZO channel for TFT applications are investigated. Results obtained from positive and negative bias stress tests are presented and discussed.

2. Experimental

The device fabrication process begins with a co-sputtering of ZrO_2 and SiO_2 targets in Ar ambient at RT to form a 9±1-nm-EOT $Zr_{0.85}Si_{0.15}O_2$ gate dielectric layer [3] on an n^+-Si substrate. Then the active channel layer was deposited by co-sputtering of IGZO and TiO_2 target in Ar ambient at RT. To control the Ti content, various powers (0, 25, 50 and 75 W) were used for the TiO_2 target with the IGZO target kept at 80 W during sputtering deposition. For comparisons, two groups of channels with and without a post-deposition annealing (PDA) at 400 °C in hydrogen (H_2) ambient for 10 min were prepared. Subsequently, a patterned 25-nm-thick Al-doped ZnO (AZO) buffer layer followed by a 200-nm-thick Titanium (Ti) metal were deposited to from source and drain (S/D) contact. Finally, a 200-nm-thick SiO_2 passivation layer was deposited via RF sputtering. The schematic cross section view of the Ti-IGZO TFTs with $Zr_{0.85}Si_{0.15}O_2$ gate dielectrics is shown in Fig. 1. All device are with a width-to-length ratio of 200 μm/20 μm.

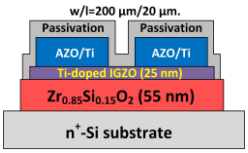

Fig. 1. Schematic of the co-sputtered Ti-IGZO TFTs with $Zr_{0.85}Si_{0.15}O_2$ gate dielectric.

3. Results and Discussion

Based on X-ray photoelectron spectroscopy (XPS), the binding energy of the O 1s peak for the Ti-IGZO films is shown in Fig. 2 and the corresponding details are listed in Table I. It indicates that amount of oxygen vacancies is decreased after Ti incorporation, because mobile electrons are liable to be captured by Ti^{4+}[1]. As shown in Figs. 2(a)-2(d), it is seen that the $O_{vac}/(O_{vac}+O_{OH}+O)$ area ratio is decreased from 32.05 % to 26.65 %, 26.69 %, and 26.72 % for sample prepared with a co-sputtering power ratio (IGZO:TiO_2) of 80:0, 80:25, 80:50, and 80:75, respectively. Note that the atomic % of Ti in these samples, based on relative sensitivity factors, are estimated to be 0%, 1.0%, 1.5%, and 2.5%, respectively, which are called type A, B, C, and D sample or channel hereafter, respectively. As shown in Fig. 2 for sample E which is the sample B with a PDA at 400 °C in N_2 for 10 min, it suggests that PDA is beneficial to suppress oxygen vacancies. Our results suggest that 1.0 % Ti-IGZO has the best film quality as compared with the others.

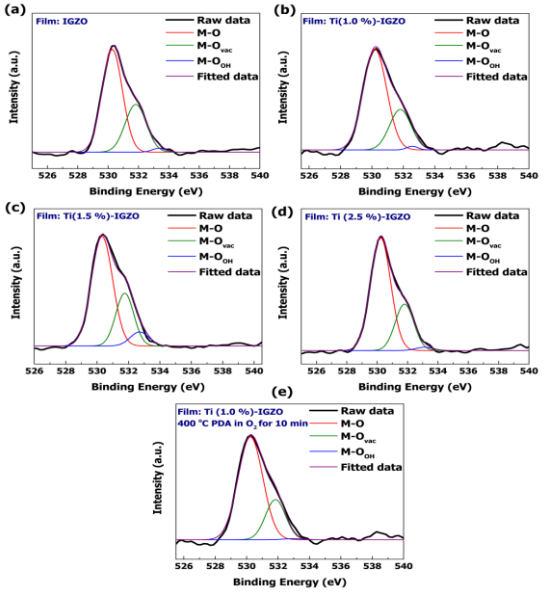

Fig 2. X-ray photoelectron spectra of O 1s peaks for Ti-IGZO thin films.

To examine the stability of the prepared Ti-IGZO TFTs, both positive (+4 V) and negative (−4 V) gate bias stress, called PGBS and NGBS, respectively, were performed and threshold voltage shift $\Delta V_{TH} (= V_{TH(stressed)} - V_{TH(initial)})$ were evaluated. Figure 3 shows the dependence of ΔV_{TH} as a function of the stress time. PGBS (NGBS) results in a positive (negative) V_{TH} shift with the magnitude increases with increasing the stress time, which is caused by electron trapping (de-

trapping) in dielectric and/or at dielectric/channel interface. It is interesting to see that the magnitude of ΔV_{TH} caused by NGBS is less than that of caused by PGBS which could be due to electron trapping rate is larger than the de-trapping rate. Note that Ti(1.0 %)-IGZO shows the best reliability among all the tested samples. Figure 4 illustrates the typical transfer characteristics of Ti(1.0 %)-IGZO TFT under PGBS and NGBS.

Table I Ti content and oxygen vacancy in Ti-IGZO films prepared by different co-sputtering power ratios

Power ratio: IGZO (W):TiO_2 (W)		Ti/(Ti+In+Ga+Zn) (%)	Symbol	$O_{vac}/(O_{vac}+O_{OH}+O)$ (%)
(Sample A)	80:0	0	IGZO	32.05
(Sample B)	80:25	1.0	Ti(1.0%)-IGZO	26.65
(Sample C)	80:50	1.5	Ti(1.5%)-IGZO	26.69
(Sample D)	80:75	2.5	Ti(2.5%)-IGZO	26.72
(Sample E)	80:25	1.0	Ti(1.0 %)-IGZO (400 °C PDA in N_2)	18.07

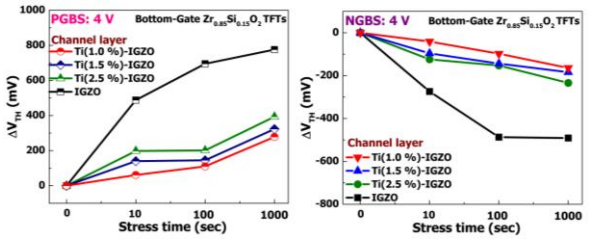

Fig. 3. Experimental ΔV_{TH} as a function of stress time for TFTs based on type A, B, C and D channel.

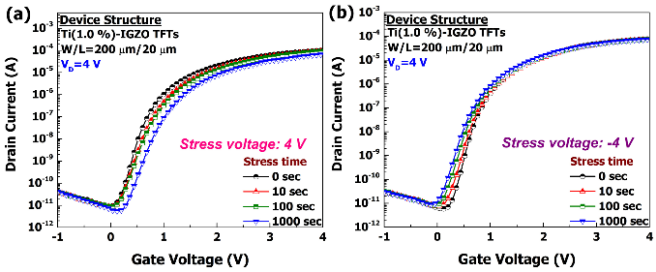

Fig 4. Effect of the stress time on Ti(1.0 %)-IGZO TFT transfer characteristics. Under stress condition of (a) PGBS and (b) NGBS.

Figure 5 shows the dependence of interface trap density (D_{it}), bulk oxygen vacancy (O_{vac}) and ΔV_{TH} as function of Ti-doped ratio. The results reveal that the Ti(1.0 %)-IGZO TFT shows the lowest values in D_{it}, oxygen vacancy, and ΔV_{TH} as compared with the other samples. It could be attributed to both D_{it} and O_{vac} are decreased by a suitable co-sputtered power ratio, which results in improved device stability. Though oxygen vacancies in Ti-IGZO Channel is decreased apparently after Ti incorporation, however, the cases with 1.5 and 2.5 % Ti content show a higher D_{it} than that of the 1.0 % Ti case. It might be due to the channel/dielectric interface is vulnerable to plasma damage with a high co-sputtering power [4]. Accordingly, the trade-off between the decrease in D_{it} and increase in plasma-related damage through increase the sputtering power for the TiO_2 target should be made with discretion.

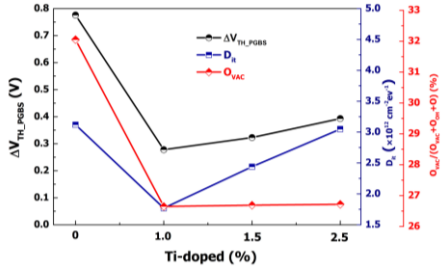

Fig 5. The dependence of D_{it}, O_{vac}, and ΔV_{TH} as function of Ti-doped ratio.

Effect of PDA at various temperatures (300, 400, and 500 °C) on the device performance of Ti-IGZO TFTs are also investigated. Figure 6 shows the transfer characteristics of Ti(1.0 %)-IGZO TFT with PDA for 10 min in N_2 at 400 °C after different stress times. As compared with results shown in Fig. 4, it reveals that ΔV_{TH} is suppressed after PDA because of reduced trap density in the Ti-IGZO channel.

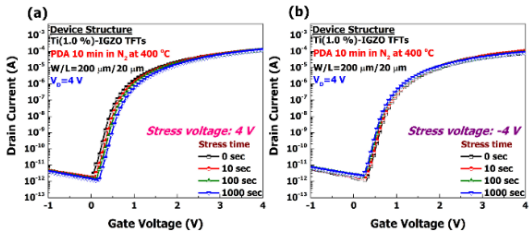

Fig 6. Ti(1.0 %)-IGZO TFT transfer characteristics with PDA in N_2 at 400 °C after (a) PGBS (b) NGBS for different stress times.

Figure 7 shows the transfer characteristics of Ti-IGZO TFTs without and with PDA for 10 min in N_2 at 400 °C. Effect of PDA on the device performance is evident. A comparison of device electrical parameters for samples prepared in this work and results reported in the literature are listed in Table II. With Ti incorporation and a suitable PDA, interface trapped density D_{it} is seen decreasing from 3.12×10^{12} to 1.09×10^{12} $cm^{-2}eV^{-1}$. Not that the suppressed D_{it} is also responsible for the improvement in SS and μ_{FE} of TFTs. Our experimental results suggests that Ti incorporation in α-IGZO channel could reduce not only the density of bulk defects but also improve the device stability for improving the quality of interface with dielectric. Ti content of around 1.0% could lead to device with the best performance in switching and reliability.

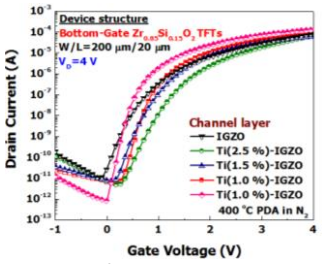

Fig 7. The transfer characteristics of Ti-IGZOTFTs without and with PDA for 10 min in N_2 at 400 °C.

Table II Comparisons of device parameters of TFTs with IGZO and Ti-doped channel

Sample	I_{on}/I_{off}	V_{TH} (V)	SS (mV/dec)	μ_{FE} ($cm^2/V\cdot s$)	D_{it} ($cm^{-2}eV^{-1}$)	ΔV_{TH} (V)
A	8.62×10^6	0.47	150	13.2	3.12×10^{12}	0.776
B	1.40×10^7	0.68	98	21.7	1.77×10^{12}	0.278
C	1.05×10^7	0.72	130	21.2	2.44×10^{12}	0.323
D	1.01×10^7	0.90	148	17.8	3.05×10^{12}	0.393
E	**1.65×10^8**	**0.40**	**90**	**24.2**	**1.09×10^{12}**	**0.157**
[5]	7.50×10^6	3.86	110	9.8	3.83×10^{12}	0.42
[6]	1.0×10^7	1.21	300	9.7	-	1.6

4. Conclusions

Ti-IGZO-TFTs with improved reliability have been successfully fabricated by co-sputtering of IGZO and TiO_2 target at RT. Our experiments show that the Ti(1.0 %)-IGZO channel could lead to a significant improvement in device reliability with reduced the threshold voltage shift from 0.776 V to 0.157 V after 1000 second PGBS and from -0.491 V to -0.093 V after 1000 second NGBS. The effectiveness of Ti incorporation in IGZO in suppressing bulk oxygen vacancy clarified in the present work confirms that Ti incorporation in IGZO channel should be very beneficial to device stability improvement.

Acknowledgements

This work was supported by the Ministry of Science and Technology (MOST) of Taiwan, under contract Nos. MOST 105-2221-E-006-196-MY3 and MOST 104-2221-E-006-130-MY3.

References

[1] Ho Yong Chong et al., Appl. Phys. Express **99** (2011) 161908
[2] H. H. Hsu et al., IEEE Electron Device Lett. **35** (2014) 87.
[3] C. H. Hung et al., Jpn. J. Appl. Phys. **56**, (2017) 04CG06.
[4] M. Kim et al., Appl. Phys. Express **90** (2007) 212114
[5] J. Raja et al., Appl. Phys. Express **102** (2013) 083505.
[6] S. Y. Sung et al., Appl. Phys. Express **96** (2010) 102107.