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An improved normally-off Al_2O_3/GaN MOSFET based on self-terminating gate-recess etching technique

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Abstract

In this letter, based on our proposed self-terminating gate-recess etching technique, an optimized normally-off Al_2O_3/GaN MOSFET was demonstrated. As a result, this fabrication technology enables flexible design of process flows and provides a good thermal management for the normally-off GaN-based MOSFETs. The fabricated devices exhibit a threshold voltage (V_{th}) of ~1.8V, a maximum drain current (I_{D_max}) of ~328mA/mm, a breakdown voltage of 218V.

1. Introduction

Normally-off recess-gated AlGaN/GaN-based MISFETs/MISHEMTs have attracted significant attention since they allow low gate leakage current, large gate swing and high threshold voltage due to the insertion of high quality gate dielectrics [1]. Cl_2-based inductively coupled plasma (ICP) dry etching technique is widely used to realize recess-gated structure. Nevertheless, such a process always suffers from poor controllability and high variability, making the recess depth nonlinear with etching time and inducing undesirable nonuniformity for device performance [2].

Previously, we proposed a self-terminating gate recess etching technique using GaN cap layer (CL) as recess mask to realize the MOSFET structures which is easy to control, highly repeatable, simple for fabrication as well as promising for industrialization [3]. However, in [3], the Ohmic formation was designed to follow the fabrication of gate recess. Thus, the high temperature annealing process in Ohmic contact formation restricts the improvement of the quality of gate dielectric (e.g. Al_2O_3) and gate dielectric/GaN (Al_2O_3/GaN) interface and might probably induce defects in Al_2O_3/GaN interface which may be the reason for the large V_{th} drift in [3]. As a result, it is of significance to develop an "Ohmic-first" self-terminating gate-recess etching technique for the fabrication of normally-off Al_2O_3/GaN MOSFETs where the Ohmic contact formation is ahead of gate-recess-etching/gate-dielectric-deposition(GRE/GDD) process.

In this letter, it is successfully demonstrated that by using Ti/Al/Ni/Au (20/160/50/150nm) metallization scheme, the source/drain Ohmic contact can endure the self-terminating gate-recess process which includes a thermal oxidation for 45min at 650℃ followed by 45min etching in potassium hydroxide (KOH) at 70℃. Thus, an optimized fabrication technology for normally-off GaN devices was achieved based on the self-terminating gate-recess etching technique. Meanwhile, the normally-off Al_2O_3/GaN MOSFETs were fabricated and characterized.

2. Device fabrication and characterization

Device fabrication

Fig.1(a) shows the devices fabrication flow, including isolation by ICP, Ohmic formation, gate recess, Al_2O_3 deposition, contact formation and gate metal. It is noted that the Ohmic formation consisting of deposition of Ti/Al/Ni/Au (20/160/50/150nm) metals and a rapid thermal annealing at 850℃ for 34s in N_2 ambient was conducted before gate recess of a thermal oxidation for 45min at 650℃ followed by 45min etching in KOH solution at 70℃ using the GaN CL as recess mask. The gate-recess depth is ~25nm measured by atomic force microscope(AFM). The Ohmic contact resistance (R_C) assessment before and after GRE is shown in Table I. Three TLM patterns located in different dies on the 1.5×1.5cm^2 sample were characterized before and after the GRE process. The results indicated that a relative good Ohmic contact was achieved without obvious degradation after the GRE process.

The schematic cross section diagram and fabrication flow of the normally-off Al_2O_3/GaN MOSFETs and detailed geometries $L_{GS}/L_G/L_{GD}$=2/2/6μm are shown in Fig. 1.

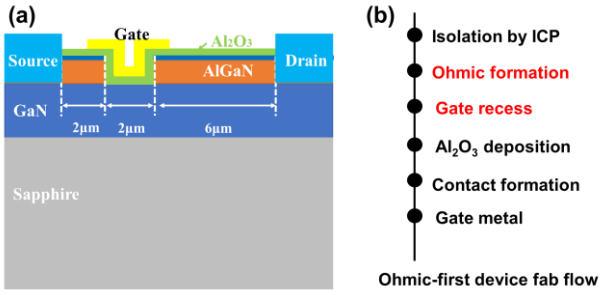

Fig.1 (a)Schematic cross-sectional diagram and (b) fabrication flow of the normally-off Al_2O_3/GaN MOSFETs based on proposed "Ohmic-first" self-terminating gate recess etching technique.

Table I The average R_C and R_{Sheet} before and after GRE process.

	Before GRE	After GRE
Average R_C (Ω•mm)	1.2	1.7
Average R_{Sheet} (Ω/□)	250	258

Device characterization

The DC transfer curves of the MOSFETs with a gate width W_G of 80μm are shown in Fig.2. The maximum drain current I_{D_max} and transconductance G_{m_max} are 328mA/mm

and 64mS/mm, respectively. Threshold voltage V_{th}, determined by the linear extrapolation method is extracted to be 1.8V. Using $\mu_{FE} = G_m L / W C_{MOS} V_{DS}$, the maximum field effect mobility (μ_{FE_max}) is 91cm^2/Vs. The obtained value is much higher than those extracted in devices fabricated using dry etching techniques which are typically ~50cm^2/Vs [4]. This result indicates that a lower damaged channel can be achieved using the proposed thermal-oxidation/KOH-etching gate recess technique. The breakdown voltage (V_{br}) is ~218V under a drain leakage current criterion of 1×10^{-4}A/mm (Fig. 3(a)). The device V_{br} can be further enhanced by improving the gate dielectric quality.

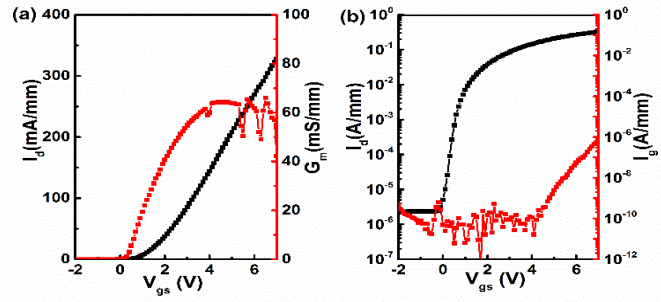

Fig.2 Transfer characteristics of the device in (a)linear and (b)log scale at V_{ds}=7V where the V_{gs} was swept from -2 to 7V.

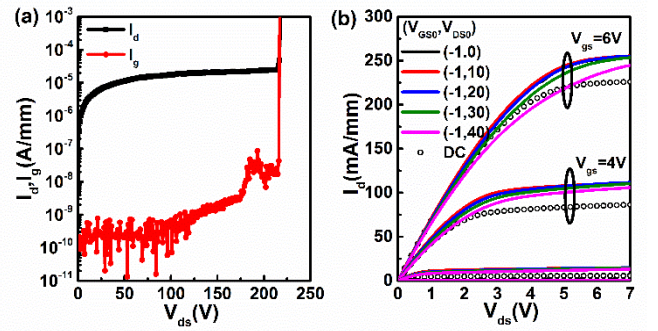

Fig.3 (a) OFF-state leakage currents of the MOSFET with the substrate floating. (b) DC and pulsed output characteristics of the MOSFET measured at different quiescent bias.

The DC and pulsed output characteristics of the fabricated device are shown in Fig.3(b) where V_{gs} changes from -2V to 6V with step of 2V. The pulsed I_d-V_{ds} curves was measured using a soft switch method [5] with different quiescent biases (V_{GS0}, V_{DS0}). The dynamic on-state resistance R_{on} extracted under the linear region at V_{ds}=1V and the dynamic drain current I_{DD} extracted under the saturation region at V_{ds}=7V are listed in Table II under the quiescent bias of (-1V, 0V) and (-1V, 40V) at V_{gs}=6V. Also, for comparison, the static R_{on} and I_{DD} determined by DC curves at V_{gs}=6V are added. Our experimental results indicated that improved dynamic R_{on} and I_{DD} are obtained under quiescent bias of (-1V, 0V) comparing with those obtained from DC curves, which could be explained by the self-heating effect. Also, under quiescent bias of (-1V, 40V), the dynamic R_{on} increased only ~9.2% while the dynamic I_{DD} decreased only ~4.1% when comparing with that obtained under quiescent bias of (-1V, 0V), suggesting that effective current collapse suppression is achieved in the fabricated device.

Table II R_{on} and I_{DD} determined by DC and pulsed IV curves

Items	DC	(-1V,0V)	(-1V,40V)	Degradation
R_{on} (Ω•mm)	14.7	14.1	15.4	9.2%
I_{DD} (mA/mm)	226	255.5	245	4.1%

3. Conclusions

In this letter, an "Ohmic first" optimized fabrication technology for normally-off GaN devices was developed based on the self-terminating gate-recess etching technique. The fabricated devices exhibit a V_{th} of ~1.8V, an I_{D_max} of ~328mA/mm, a V_{br} of 218V, and a gentle current collapse. This proposed technology enables a flexible fabrication flow and provides a better thermal management of gate dielectric and gate dielectric/GaN interface quality when further enhancing the device performance.

Acknowledgements

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