PS-6-11

Electrical Performances of 1T-DRAM based on PNPN Tunneling FET with asymmetric Double-Gate Structure

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Abstract

This paper presents an electrical performances of 1T-DRAM based on PNPN tunneling FET with asymmetric double-gate structure. The materials of the source, the channel, and the drain regions are P-type Ge, P-GaAs channel, and N-type drain, respectively. The N-doped layer for an improved current drivability was inserted between the Ge-source region and the GaAs-channel region. It is observed that the proposed 1T-DRAM have 2.9 times larger current margin and 1.4 times longer retention time than a 1T-DRAM with the conventional TFET.

1. Introduction

A cell of the conventional dynamic random access memory (DRAM) is composed with one-transistor and one-capacitor (1T-1C). Unfortunately, the fabrication technology for the cell capacitor in DRAM is faced with the limit such as high aspect ratio structure and non-uniform dielectric deposition. To overcome these problems, a capacitorless 1T-DRAM has been proposed and studied by many research groups [1-4].

Recently, the tunneling field-effect transistors (TFETs) have been studied as a promising candidate for 1T-DRAM. However, the TFET-based 1T-DRAMs have small current margin due to low TFET's current [5, 6]. As a solution for improving the TFET's current, the application of Ge/GaAs heterojunction to the TFET has been proposed. Moreover, the Ge/GaAs TFET is known as the devices with steep subthreshold current characteristics and high on-/off-current ratio [7, 8]. In this work, we perform the simulation for 1T-DRAM based on PNPN TFET with Ge/GaAs heterojunction [10]. To enhance the current-margin and the retention time (RT), an N-doped layer is applied to the tunneling region. The simulation work was conducted in Sentaurus program [9].

2. Device structure and simulations

Figure 1 shows the cross-sectional view of the proposed 1T-DRAM. The doping concentrations of the source, the drain, and the channel regions are P-type 5×10^{19} cm^{-3}, N-type 5×10^{19} cm^{-3}, and P-type 1×10^{16} cm^{-3}, respectively. The GaAs N-type layer between the Ge source and the GaAs channel plays a role to improve the tunneling rate and its doping-concentration is fixed to 6×10^{18} cm^{-3}.

For the accurate simulations, we include Shockley-Read-Hall recombination model, doping-dependent mobility model, trap-assisted-tunneling model, and non-local band-to-band tunneling model in our simulation [9]. Because the valence band edge (E_v) of Ge-source region and the conduction band edge (E_c) of GaAs-channel region are aligned at the same value in k-space (k = 0), the direct tunneling is dominant in the proposed 1T-DRAM [10]. Therefore, we adopted the direct BTBT process in this work.

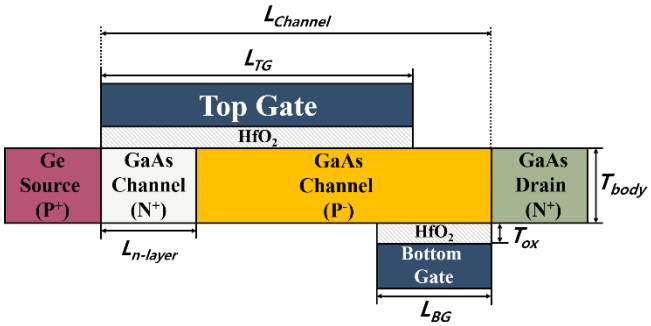
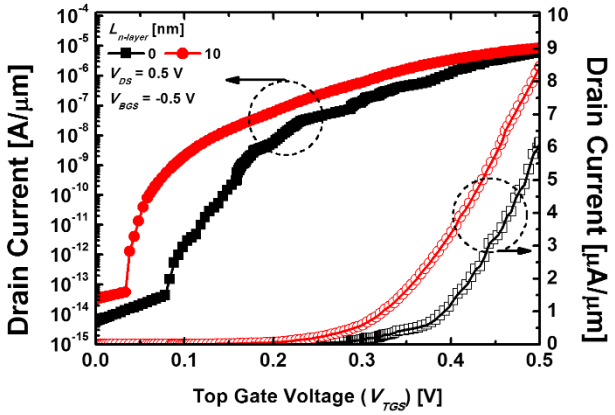


Fig. 1 Device Structure of Ge/GaAs PNPN TFET-based 1T-DRAM

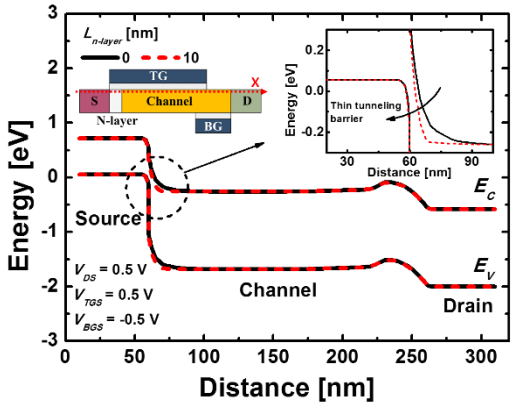
3. Results and discussion

The electrical characteristics of the proposed Ge/GaAs PNPN TFET-based 1T-DRAM have been investigated as shown in Fig. 2(a) and 2(b). The proposed device has 160 nm-long top-gate, 60 nm-long bottom-gate, 30 nm-thick body, and 2 nm thick HfO_2 gate-dielectric. The tunneling current flows under the top-gate. The bottom gate voltage plays a role to collect many hole-charges in P-type GaAs channel region under the bottom-gate. From Fig. 2(a) and 2(b), we confirm that the thinning of the tunneling barrier due to N-type layer results in boosting the on-state current. Therefore, it is expected that the proposed 1T-DRAM have the improved memory performances.

In 1T-DRAM, the excess majority carriers in the body make state '1' and increase the on-state current of a TFET. The charge storage region of the proposed 1T-DRAM is the body region under the bottom-gate made by high workfunction material. On the other hand, the top-gate is used the conventional gate electrode of the transistor. The state '1' operation is obtained by applying a negative bias to the bottom-gate to form a hole storage region (V_{TGS} = 0.5 V, V_{BGS} = -0.5 V, V_{DS} = 1.0 V). In contrast, the positive bottom-gate voltage results in the state '0' owing to the removal of hole charges (V_{TGS} = -1.0 V, V_{BGS} = 2.5 V, V_{DS} = 2.5 V). The positive charges in the hole storage region make a threshold voltage (V_{th}) of TFETs, and thus, the tunneling current increases at the state '1'.



(a)



(b)

Fig. 2 The Electrical characteristics of the proposed 1T-DRAM. (a) I_{DS}-V_{TGS} curves. (b) Energy band diagram for region under the top gate electrode.

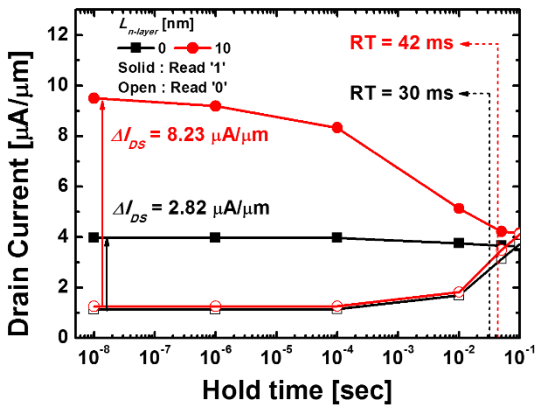


Fig. 3 Memory performance of Ge/GaAs DG TFET 1T-DRAM depending on the thickness of N-doped boosting layer.

Figure 3 shows the drain currents at the state '1' and state '0' as a function of the hold time. The current margin is defined at the difference between the read '1' current and the read '0' current. As shown in Fig. 3, the recombination of holes in the storage region makes the current margin small as the hold time increases. To recover lost charges, the DRAM needs the refreshing operation with the inevitable power consumption. The refreshing interval time must be long for low-power consumption. The RT of DRAM mean the hold time that is able to hold the data without the refreshing operation. Therefore, the RT is the main figure-of-merit of 1T-DRAM. In this work, the RT is obtained as the hold time at the current margin of 1 μA/μm [11].

From Fig. 3, the maximum current margin of the proposed PNPN TFET-based 1T-DRAM is 8.23 μA/μm. And the RT is 42 ms and it is 40%-larger than that of 1T-DRAM based on PPN TFET. These results indicates that applying the N-layer could be a solution for the enhanced TFET-based 1T-DRAM by enhancing the drain current margin.

4. Conclusions

In this work, we performed Ge/GaAs PNPN TFET-based 1T-DRAM with an n-doped boosting layer by TCAD simulations and analyzed its memory performances. The n-layer improved the tunneling probability and on-state current. Then, the drain current margin increased about 2.9 times (8.23 μA/μm) and retention time was enhanced about 1.4 times (42 ms) compared with 1T-DRAM based on the conventional TFET.

Acknowledgements

This work was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science, ICT & Future Planning (2016R1C1B2015979), and in part by Samsung Electronics Co. Ltd. This work was supported by the BK21 Plus project and Global Ph.D. Fellowship Program through the NRF funded by the Ministry of Education (21A20131600011, 2013H1A2A1034363). This work was supported by IDEC (EDA Tool, MPW).

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