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Transient-mode Simulation of MOS C-V Characteristics for GaN

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Abstract

GaN MOS C-V device simulations considering various types of interface and bulk traps are performed by transient-mode. The simulations explain various features of C-V curves, such as plateau, hysteresis, frequency dispersions which are arising from the complicated combinations of interface and bulk deep level traps. The present method is a good theoretical tool to understand the physics behind various un-ideal C-V measured curves.

1. Introduction

GaN MOSFET is actively studied to enable higher speed, higher power devices [1]-[4] beyond silicon technologies. Recently good MOS *C-V* characteristics are reported [5], but it is still limited and has some restrictions. Such un-ideal *C-V* characteristics are occurring caused by bulk and interfacial deep level traps. From experimental points of view, it is hard to distinguish such *C-V* non-ideality without any theoretical tools. In this work, transient device simulation is used with deep level trap models to obtain MOS *C-V* characteristics, and discusses cases of non-ideal *C-V* curves which are typically observed in measurements.

2. Simulation Method

Carrier generation and recombination mechanisms arising from the deep level interface and bulk traps are implemented into the classical semiconductor device simulator Hy-ENEXSS [6]. *C-V* characteristics of MOS capacitors with various conditions are calculated by transient simulation as shown in Fig.1. To obtain better convergence, carrier generation and recombination rates are calculated by considering the changes of ionized trap densities during each time step. This stabilizes the simulation convergence for wide range of time scales.

The time scale of the electron behaviors governed by the deep level acceptor trap is determined mainly by the carrier emission rate E_n described by

$$E_n = v_{th}\sigma_n N_C exp(-q\Delta E/k_B T),$$

where v_{th} is the thermal velocity, σ_n is the capture cross section, N_C is the effective density of states of the conduction band, and ΔE is the trap energy depth below the conduction band minimum. The time scale which is the inverse of this emission rate E_n for GaN electrons is shown in Fig. 2 for the guideline to understand the simulation results in this paper. The electron capture cross section σ_n of the trap is assumed to be 10^{-14} cm^2, for all the simulations throughout this work.

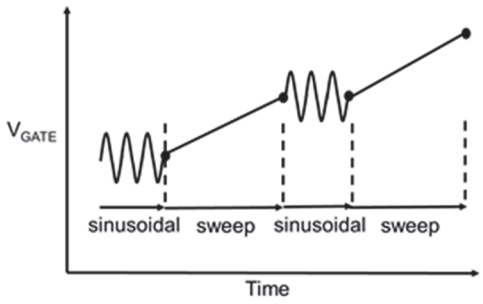

Fig. 1 *C-V* curves are simulated using transient model.

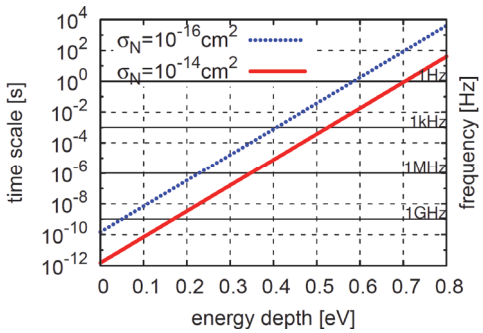

Fig. 2 Time scale vs energy depth of GaN electrons..

3. Results

Interface Traps

Fig. 3 shows GaN MOS *C-V* curves with 15nm effective oxide thickness (EOT), n-type 5×10^{16} /cm^3 substrate, and the acceptor trap with energy depth 0.5 eV below the conduction band. Several lines correspond to different interface trap densities, where CV-shifts and plateau are observed. The markers are for bulk trap distributed from the surface to 0.1 μm depth, adjusting the area density to 10^{12} /cm^2. The C-V slope of the bulk trap around the flat-band differs from the ideal curve.

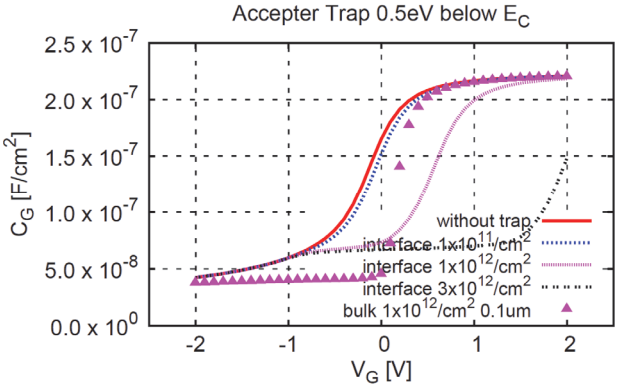

Fig. 3 *C-V* curves of GaN MOS with different trap densities.

Fig. 4 shows the frequency dispersion of the C-V curves. In this figure, the energy level of the trap is assumed to be a δ-function located at 0.5 eV. As shown in Fig. 2, the time scale for 0.5 eV is under the 1 msec., which corresponds to the frequency peak of 3 kHz.

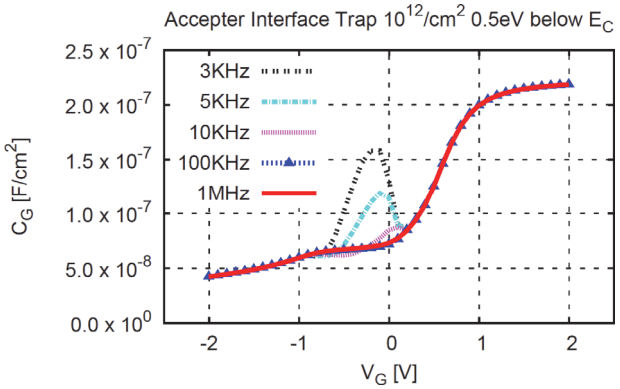

Fig. 4 The frequency dispersion of the *C-V* curves for interface trap of 10^{12}/cm^2.

Fig. 5 shows the *C-V* characteristics for different trap energy dispersion σ_E. The trap energy peak is fixed again to 0.5 eV and the *C-V* frequency is 100 kHz. When the energy dispersion becomes wider, the shallower energy traps contribute to the frequency dispersion of 100 kHz. Compared to Fig. 4, more capacitances are observed between the capacitance peak and the accumulation capacitance, as typically observed in the measurements [5].

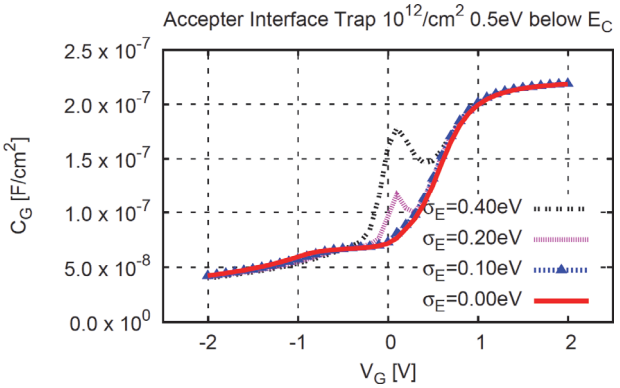

Fig. 5 *C-V* characteristics for different trap energy dispersion values σ_E. The trap energy center is fixed to 0.5 eV below the conduction band, and the frequency is 100 kHz.

Frequency Dispersion in Strong Accumulation

Fig. 6 shows the *C-V* characteristics for higher substrate resistivity corresponding to substrate carrier density of 6×10^{12} /cm^3 and 100 μm thickness. In such a situation, frequency dispersions are observed in the strong accumulation region, which are also often observed in the measurements.

Hysteresis

Fig. 7 shows the *C-V* hysteresis characteristics for interface trap whose energy is 0.6 eV below the conduction band by changing the voltage sweep speed. Thus the measurements should be carefully set up to exclude such slow phenomena concerning the deep traps.

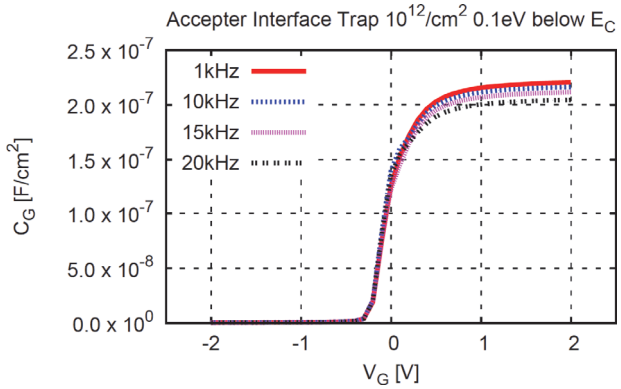

Fig. 6 In higher substrate resistance cases, frequency dispersions in the strong accumulation region are observed.

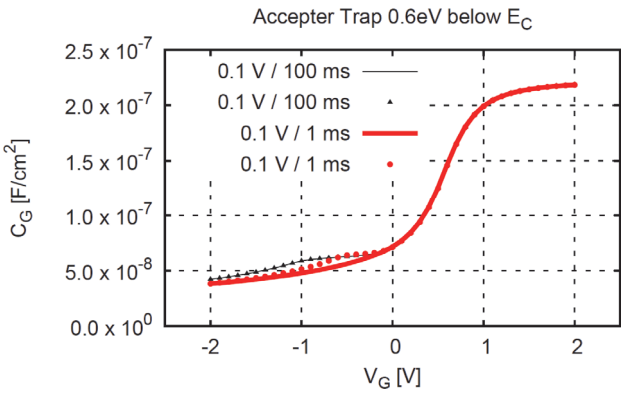

Fig. 7 Hysteresis characteristics by changing the voltage sweep speed. The frequency is 10 MHz.

3. Conclusions

GaN MOS capacitors with bulk and interface deep level traps are simulated by transient-mode, which successfully explains *C-V* shifts, plateau, frequency dispersions, and hysteresis characteristics. The simulation can be widely used to discuss the effects of the trap energy dispersions, voltage sweep speed, substrate resistances, and combinations of different traps. The present method is a strong tool to quantitatively evaluate the measured *C-V* curves which include complicated deep trap information.

Acknowledgements

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References

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