PS-9-06

A Vertical Ge Tunneling FET with Tapered Source/Drain Strctures

Kehuey Wu[1], Guang-Li Luo[1,*], Chun-Lin Chu[1], Shih-Hong Chen[1], Bo-Yuan Chen[1],
Wen-Fa Wu[1], Wen-Kuan Yeh[1,2], and Chao-Hsin Chien[3]
[1]National Nano Device Laboratories, NARL, Hsinchu, Taiwan (*E-mail: glluo@narlabs.org.tw)
[2]Dept. of Electrical Engineering,National University of Kaohsiung, Kaohsiung, Taiwan
[3]Dept. of Electrical Engineering,National Chiao-Tung University, Hsinchu, Taiwan

Abstract

A novel Ge sandglass-shaped vertical tunneling FET (SVTFET) was proposed and experimentally demonstrated. The further simulation shows that minimal S.S. about 20mV/dec and I_{on}/I_{off} >10^6 can be achieved with channel length L_g=40nm and wire width W=20nm. Due to tapered S/D, the S/D series resistance of SVTFET is much smaller than that of conventional nanowire TFET (NWTFET). With tapered S/D, SVTFET can be further scaled down to Lg=10nm (as illustrated in Fig. 1) with minimal S.S. of 38mV/dec and on current (I_{Dsat}) of 48μA/μm at V_G=V_D=0.5V.

Introduction

TFETs have been extensively studied due to its potential for achieving S.S.<60mV/dec such that the supply voltage can be lowered [1]. Additionally, because of its smaller bandgap, higher mobility, and the possibility of strain engineering a direct-gap TFET, Ge or GeSn is considered an excellent candidate for further performance improvement [2,3]. In the present work, a novel Ge SVTFET is proposed and explored. First, the detailed manufacturing process will be explained. The electrical characteristics of fabricated devices will be presented and used to calibrate the simulation parameters. The TCAD device simulation [4] was then applied to study the scaling capability of SVTFETs.

Device Fabrication and Device Characterization

A. Device Fabrication

The fabrication process of SVTFET is shown in Figs. 2 and 3. An *in-situ* doped Ge PIN structure was first epitaxially grown by a LPCVD system at 400°C. The sandglass-shaped vertical structure was then formed by dry-etching and subsequent anisotropic wet-etching in H_2O_2 solution. The side gate stack comprises an RTO GeO_2 interfacial layer, an ALD Al_2O_3 high-k layer and a sputtered TiN metal film. The electrical isolation between the side wall TiN gate and the top TiN drain contact is automatic as a result of the etched undercut of top TiN. A SVTFET structure is shown in Fig. 4. The isolation between gate and drain electrodes was verified, and the leakage current was below pA (Inset in Fig. 4(b)). **This device has advantages of low series resistance, sub-lithography-limit channel (or wire) width by anisotropic etching, ultra-low probability of threading dislocation penetration due to channel region necking.**

B. Device Characterization

Fig. 5 depicts the TEM image of a completed device. The p-type doping in source is estimated to be $3\times10^{19}cm^{-3}$, while the n-type doping in drain is approximately $1\times10^{19}cm^{-3}$. Fig. 6 shows the I_DV_G characteristics for V_D=0.5V at different temperatures between 233K and 298K. At lower V_G, the subthreshold current is temperature dependent. However, at higher V_G, the drain current is almost temperature independent, as expected of band-to-band tunneling (BTBT). Fig. 7 shows the Arrhenius plots of I_D at V_D=0.5V for different V_G. It indicates that carrier transport is driven by trap assisted tunneling (TAT) at low V_G, and direct BTBT at high V_G.

Device Simulation, Short Channel Effects, and Scaling Capability

A. Device Simulation

To further explore Ge SVTFETs, device simulations [4] are performed. In Fig. 8, two sets of experimental data measured at 298K and 233K and one set of simulation data simulated at 298K are compared. The simulated device structure (Fig. 9) was constructed using Sentaurus Structure Editor (SDE) based on the TEM picture in Fig. 5. As can be seen, the experimental data measured at 233K with suppressed TAT are very close to the simulation result. This indicates that if the defects (ex. high-k dielectric D_{it}) can be further reduced, the device behavior can be well predicted by simulations. It was also observed that, at medium V_G=1.5V-2.5V, the simulated I_{Dsat} almost matches the experimental data. At higher V_G=2.5V-3.0V, the experimental I_{Dsat} exhibited a little lower value than the simulated one. This is probably due to the large contact resistance between TiN/n^+-Ge.

B. Short Channel Effects

Based on the results explained above, Ge SVTFETs are further investigated by simulating a device (Fig.10) with wire width W=20nm, EOT=1.0nm, and various L_g to examine the impact of short channel effects (SCEs). As shown in Fig. 11, for L_g=80nm and 40nm, the min. S.S. can be kept at about 20mV/dec. If the L_g is reduced to 20nm, the I_{off} increases by more than two orders of magnitude and the min. S.S. rises to well above 60mV/dec. This result points out that, in order to have a well-behaved tunneling FET, the SCEs need to be tightly controlled like the planar CMOS.

C. Scaling Capability

The scaling capability of Ge SVTFET is also examined by simulations. The Ge SVTFET shown in Fig. 10 is compared with the conventional Ge NWTFET (Fig. 12). Both devices have L_g=10nm, and EOT=1Å. Fig. 13 shows the simulation results of I_DV_G characteristics with W as the variable. For sufficiently thin W, the SVTFET provides smaller S.S. and higher I_{Dsat} than NWTFET due to better short channel control and smaller S/D series resistance. Fig. 14 shows band diagram of SVTFET with W=2nm and 6nm at V_D=0.5V and V_G=0V and 0.5V. The tunneling barrier width of W=2nm is smaller than W= 6nm device, which results in larger I_{Dsat}. In addition, W=2nm also has better short control, which results in smaller S.S. and I_{off}. Figs. 15 (a) and (b) summarize the S.S. and I_{Dsat}, respectively. Due to the SCEs, W needs to be aggressively thinned down to achieve low S.S. Here the superior sandglass shape (low series resistance) shines. The I_{Dsat} of SVTFET increases as W decreases. In contrast, for the NWTFET, I_{Dsat} decreases. This can be attributed to increased S/D series resistance as W decreases.

Conclusion

A novel Ge SVTFET is proposed and explored. The device is formed by *in-situ* doped epitaxy and anisotropic etching processes. To ensure a steeper S.S., SCEs must be well controlled by aggressively scaling the wire width. With the superior sandglass shape, SVTFETs can be scaled to L_g=10nm and still has excellent S.S. of 38mV/dec and I_{Dsat} of 48μA/μm at V_G=V_D=0.5V due to the ultra-low series resistance. This structure is therefore promising for nano-scale high performance tunneling FETs.

References: [1] A. Seabaugh and Q. Zhang, Proceedings of the IEEE, pp. 2095-2110, 2010. [2] Y. Yang *et al.*, IEDM, p.379, 2012. [3] T. Krishnamohan *et al.*, IEDM, p.947, 2008. [4] Sentaurus Device User Guide, Version G-2012.06.

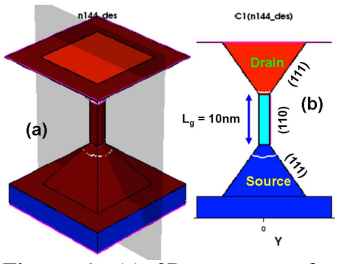

Figure 1. (a) 3D structure of SVTFET with L_g=10nm. (b) Cross-section of the device.

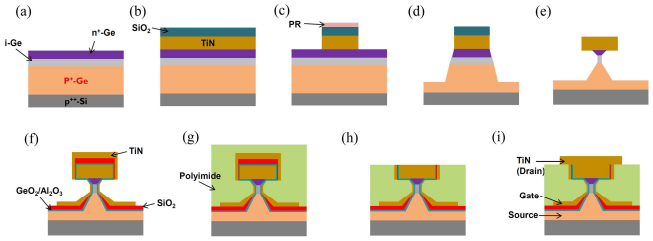

Figure 2. Schematic of the device fabrication of Ge SVTFET.

- (a) LPCVD Epi of *in-situ* doped Ge PIN structure on Si
- (b) TiN and SiO_2 deposition
- (c) E-beam litho., SiO_2 and TiN dry-etching
- (d) Ge dry-etching to form the vertical PIN structure
- (e) Ge channel shrinking by anistropic wet-etching. A sandglass shape formed.
- (f) GeO_2+Al_2O_3 gate oxide, SiO_2 field oxide, TiN gate metal
- (g) Polyimide spin-coating, and hard curing
- (h) Etch-back of polyimide, top residual TiN and SiO_2
- (i) Final TiN drain-side metal contact formation

Figure 3. Process flow of the Ge SVTFET.

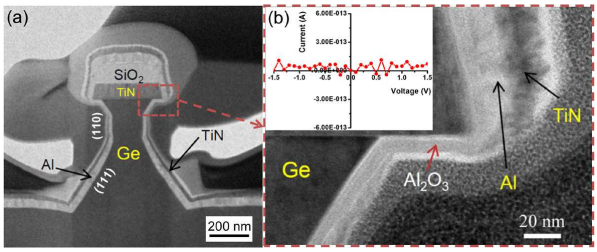

Figure 4. (a) TEM image of a Ge PIN structure with taped S/D ; (b) Zoomed in image and isolation test (inset) between the side gate TiN and top drain TiN.

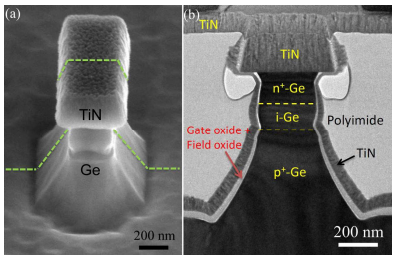

Figure 5. (a) SEM image of wet-etched Ge with TiN contact. (b) Cross-sectional TEM image of a completed Ge SVTFET.

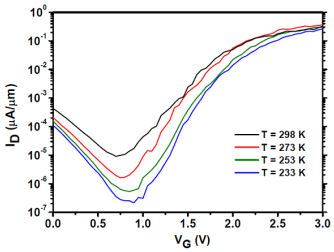

Figure 6. The I_DV_G measured at different temperatures between 233K and 298K. V_D=0.5V.

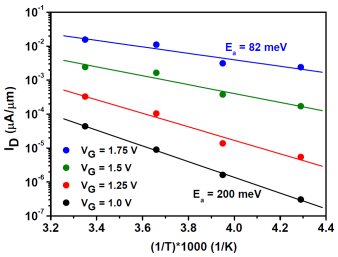

Figure 7. Arrhenius plots of I_D at V_D=0.5V and various Vg. The activation energy E_a for the lowest and highest V_G is labeled.

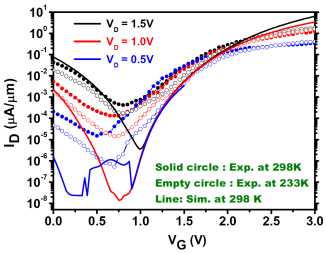

Figure 8. Comparison of experimental and simulated I_DV_G for the device shown in Fig. 5(b). (simulation structure shown in Fig. 9)

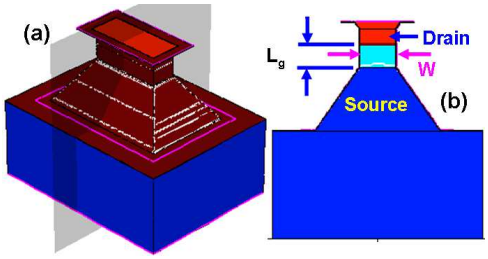

Figure 9. (a) Simulated 3D structure of the SVTFET emulating the device shown in Fig. 5(b), and (b) the cross-section of the device.

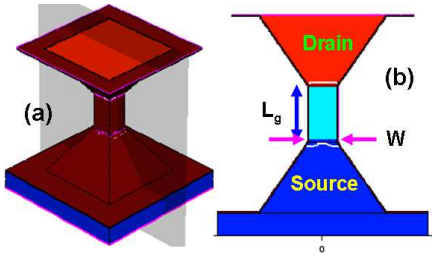

Figure 10. (a) 3D structure of simulated SVTFET. (b) Cross-section of the device.

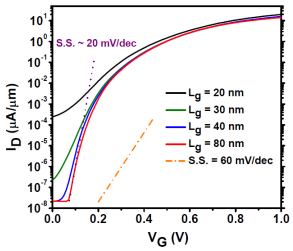

Figure 11. Simulated I_DV_G of the SVTFET in Fig. 10. V_D=0.5V.

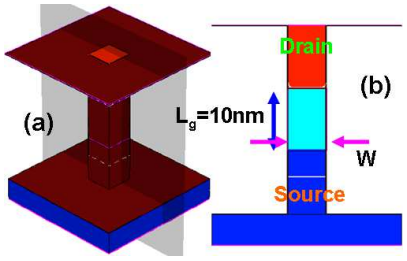

Figure 12. (a) NWTFET without tapered S/D. (b) Cross-section of the NWTFET.

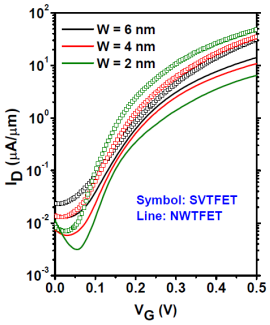

Figure 13. Simulated I_DV_G characteristics of SVTFET and NWTFET. V_D=0.5V.

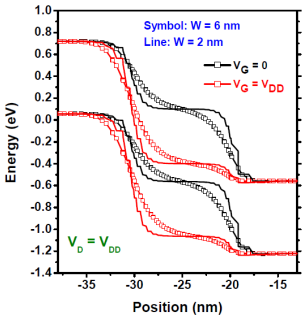

Figure 14. Band diagram of SVTFETs at V_D=0.5V and V_G=0V and 0.5V.

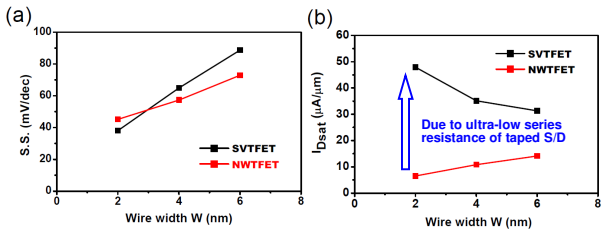

Figure 15. (a) Plot of min. S.S. vs. W. As W is thinned down, the min. S.S improves. (b) For SVTFET, I_{Dsat} increases as W decreases. However NWTFET shows an opposite trend, due to increased S/D series resistance.