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Device Performance and Characteristics of Nano Scale n-type Junctionless FET (nJLFET) with Raised Source and Drain Structure

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1. Instructions

As CMOS device continuing scaling bellow 22 nm technology node, the traditional inversion mode MOSFET device requires the ultra-sharp source and drain junction in channel region [1]. Due to the PN or (NP) junction needs some distance to achieve the anti-type doing between the source/drain and channel region, and this leads to the large channel length variation [2-4]. In addition, the nanoscale device needs ultra-shallow S/D junction to reduce the parasitic series source/drain resistance (R_{SD}) [5,6]. These issues can be overcome by the junctionless FET (JLFET) with the same type doping in channel and source/drain region [2,3]. And the JLFET displays the simple device process, less channel length variation, and lower thermal budget that is no source/drain doping annealing [7,8]. Thus, the JLFET is one of the most promising candidates for the next generation of CMOS device application [9]. But, the JLFET is turned off by the depletion region in channel underneath the gate electrode. This depletion is formed by using the work function difference between the gate and Si-channel to achieve the positive (negative) threshold voltage for n-type (p-type) JLFET [7]. Large work function difference of gate electrode and the thinner Si-channel are required to finish the superior device performance. However, the thin channel thickness will increase the R_{SD} and to degrade the device performance. Some reports have been investigated these problems [10-12], but the drain current and the I_{ON}/I_{OFF} ratio are not very well, or the I_{OFF} current is large. In this study, we investigates the n-type JLFET (nJLFET) with raised source/drain and with extra same type higher doing. The effects of gate spacer capping are studied to improve the device performance. Finally, the short channel and narrow width effects are also studied.

2. Experimental

A 6-in p-type Si wafer is used for the nJLFET device fabrication. After the RCA cleaning, the buried oxide (200 nm) (BOX) and LPCVD Si_3N_4 (50 nm) were formed. Then, the amorphous Si (50 nm) was deposited and to form the Poly-Si channel by the solid phase crystallization (SPC) at 600ºC/24 hrs. N-type channel doping of phosphorus ions with 5×10^{14} dose/cm^2, 10 keV and the RTA process. The active area was defined by the E-beam lithography and RIE etching. Then the 2nd E-beam lithography to define the channel region and to thin down the channel thickness to 20 nm. The area of channel without etching is the raised source and drain region. The gate dielectric is the 3.5 nm Al_2O_3 deposited by the ALD. The metal gate is TiN (50 nm) deposited by a PVD. The gate area is defined by the 3rd E-beam lithography, and the extra higher same type source/drain doing is using the arsenic (As) ions with 1×10^{15} dose/cm^2, 10 keV. The gate spacer is deposited by the PECVD SiO_2 and RIE etching. The JLFET without spacer is also prepared for the comparison. Finally, the Al-Si-Cu metal (200 nm) was deposited by the PVD as the contact metal. The schematic of nJLFET and the detail device process are shown in **Fig. 1** and **Fig. 2**, respectively.

3. Results and Discussion

Fig. 3 and **Fig. 4** show the Id-Vgs and Id-Vds curves, respectively, of nJLFETs w/ and w/o raised S/D for the device with gate spacer and W/L= 40/80 nm. The raised S/D nJLFET reveals the better performance with lower off current and V_{th}, better SS and larger Ids. Obvious larger Ids current of nJLFET at the liner region as sown in **Fig. 4b**, indicating the lower parasitic R_{SD} for the raised S/D nJLFET. **Fig. 5** shows the comparison of the nJLFET w/ and w/o raised S/D. Lower off current, better SS and larger Ids at 2.0V are observed in the **Fig. 5a**, and the Ids is increased by 2.54 times (at Vds=2.5V) shown in **Fig. 5b** for the nJLFET with raised S/D structure. **Fig. 6** shows the Id-Vgs curves of the raised S/D nJLFETs without the gate spacer capping. In compared with **Fig. 3b**, the nJLFET without gate spacer reveals the larger I_{OFF} and worse SS. **Fig. 7** shows the comparison of Id-Vgs and Id-Vds of the raised S/D nJLFET w/ and w/o gate spacer capping. The I_{ON} and I_{OFF} are both smaller for the nJLFET with gate spacer capping (**Fig. 7a**). In addition, the Ids is decreased by the 0.64 times (at 2.5V) (**Fig. 7b**). Thus, the gate spacer capping decreases the I_{ON} current, but it obviously decreases the I_{OFF}, thus, the ratio of I_{ON}/I_{OFF} is increase than that of nJLFET without the gate spacer capping. Additionally, the spacer capping increases the channel resistance at the liner region (**Fig. 7b**). Presumably, the RIE etching to form the gate spacer will decrease (over etch) the channel thickness and to increase the parasitic R_{SD} resistance.

Fig. 8, **9**, **10**, and **11** show the short channel and narrow width effects (SCE and NWE) on the V_{th}, SS, DIBL, and I_{ON}/I_{OFF} ratio, respectively, for the nJLFETs with various structures. The raised S/D nJLFET with spacer reveals the less SCE for the V_{th}, SS, and the superior DIBL for the NWE (Fig.10b). In addition, the raised S/D nJLFET with gate spacer presents the superior I_{ON}/I_{OFF} ratio (Fig.11). **Table I** shows the summary of the device performance of various nJLFETs structures with W/L= 40/80 nm. **Table II** shows the summary of the I_{ON}/I_{OFF} ratio of various nJLFETs devices with different channel lengths. According to the results of the Table I and Table II, the optimal device structure and the superior device performance is the nJLFET with raised S/D and with gate sidewall spacer capping.

4. Conclusions

This work investigates the characteristics of the nJLFET w/ and w/o raised source/drain structure, and the effects of gate spacer capping. In summary, the nJLFET with the raised S/D and the gate spacer capping revels the superior performance. Additionally, there is obvious improvement on the short channel effects of the devices.

Acknowledgements

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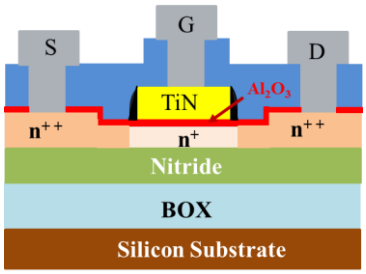

Fig.1 Schematic of n-type channel Junctionless FET (JLFET) transistor with raised source/drain and gate spacer.

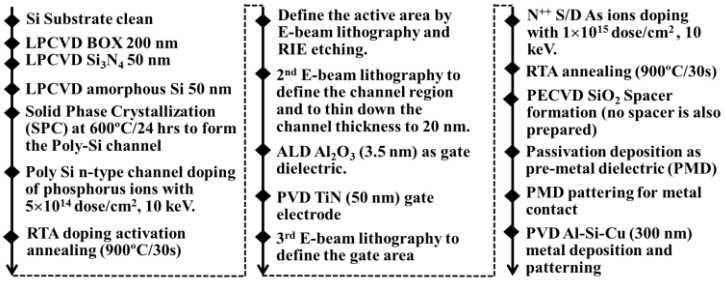

Fig.2 Fabrication process and deposition conditions for the n-type JLFETs with raised source/drain and gate spacer. Without raised S/D or without gate spacer JLFETs are also prepared for the comparison.

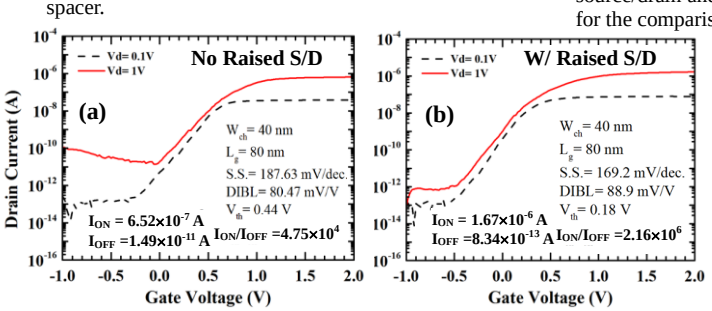

Fig.3 Id-Vgs curves of nJLFETs (a) without raised S/D, (b) with raised S/D region at Vds = 0.1 and 1.0V. The nJLFETs have the gate spacer and the W/L = 40/80 nm.

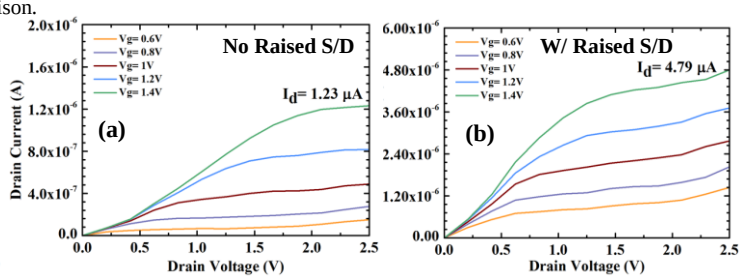

Fig.4 Id-Vds curves of nJLFETs (a) without raised S/D region, (b) with raised S/D region at various Vgs voltages. The nJLFETs have the gate spacer capping and the W/L = 40/80 nm.

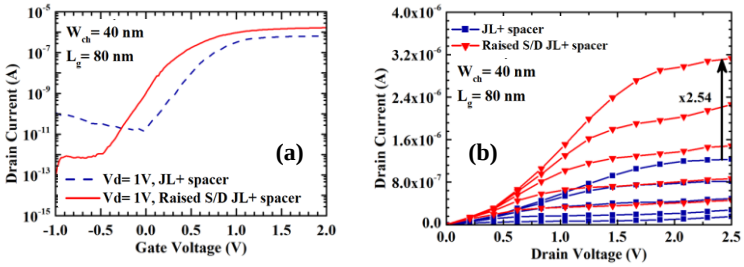

Fig.5 (a) Id-Vgs and (b) Id-Vds of nJLFETs w/ and w/o raised S/D structure for the comparison. The nJLFETs have the gate spacer capping and the W/L = 40/80 nm.

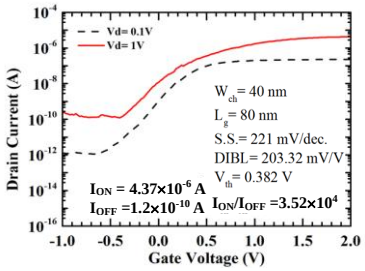

Fig.6 Id-Vgs curves of the raised S/D nJLFETs without the gate spacer capping. The device dimension is W/L = 40/80 nm.

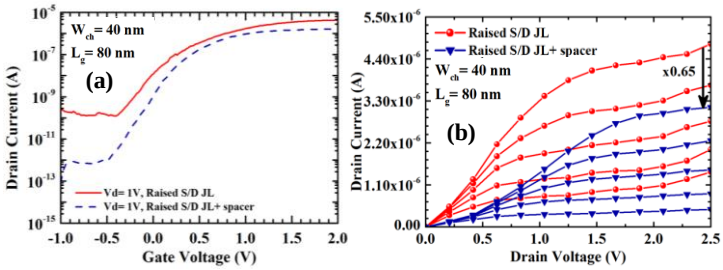

Fig.7 (a) Id-Vgs and (b) Id-Vds curves of the raised S/D nJLFETs w/ and w/o the gate spacer capping for the comparison. The device dimension is W/L = 40/80 nm.

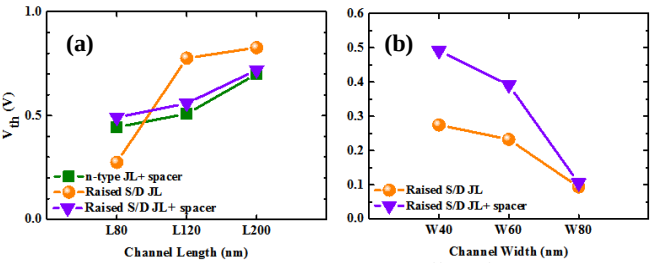

Fig.8 (a) short channel and (b) narrow width effect of threshold voltages of nJLFETs with the raised S/D or gate spacer structures for the comparison.

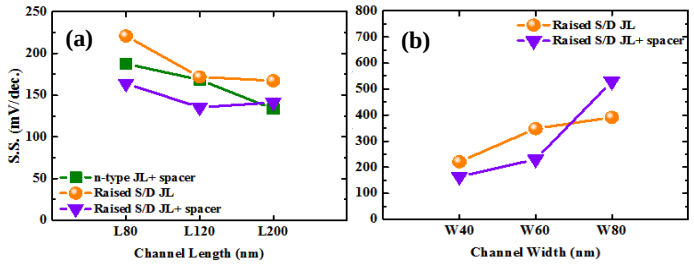

Fig.9 (a) short channel and (b) narrow width effect of subthreshold swing (SS) of nJLFETs with the raised S/D or gate spacer structures for the comparison.

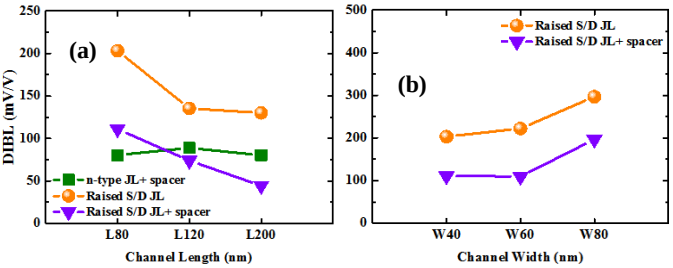

Fig.10 (a) short channel and (b) narrow width effect of drain induced barrier lowering (DIBL) of nJLFETs with the raised S/D or gate spacer structures for the comparison.

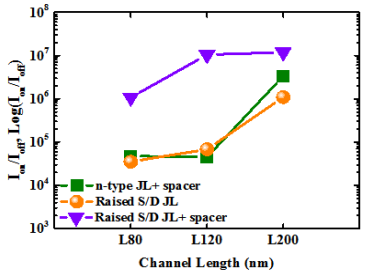

Fig.11 I_{ON}/I_{OFF} ratio of nJLFETs with the raised S/D or gate spacer structures at different gate lengths for the comparison.

Table I Device performance of various nJLFETs structures for the W/L= 40/80 nm.

nJLFET Performance	nJLFET+ Spacer	nJLFET+Raised S/D (No spacer)	nJLFET+Raised S/D+Spacer
SS (mV/dec)	187	221	169.2
DIBL (mV/V)	80.47	203.32	88.90
I_{ON}/I_{OFF}	4.75E+04	3.52E+04	2.16E+06
Idsat (μ A)	1.23	4.79	3.13

Table II I_{ON}/I_{OFF} ratio of various nJLFETs devices with different channel lengths.

Device Types	Device ON/OFF ratio (I_{ON}/I_{OFF})		
Wch = 40 nm	Lg = 80 nm	Lg = 120 nm	Lg = 200 nm
nJLFET+Spacer	4.75E+04	4.50E+04	3.35E+06
nJLFET+Raised S/D (No spacer)	3.52E+04	6.81E+04	1.09E+06
nJLFET+Raised S/D +Spacer	2.16E+06	1.05E+07	1.19E+07