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Low-power, Forming-free and Analog-type Resistive Switching in Pt/SiO_x/ZnO/Pt Oxide Heterostructures as an Electronic Synapse

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Abstract

We report an electronic synapse based on resistive switching (RS) phenomena and Schottky-like contacts in Pt/SiO_x/ZnO/Pt stack oxide heterostructures. Necessities such as low-power, forming-free, good dynamic window, long-durability and important analog-type RS behavior were all observed and discussed.

1. Introduction

Increasing worldwide research activity in brain-related projects brings out a new era of brain-inspired computing [1]. So-called neuromorphic computing requires small, low power and highly efficient basic elements such as neurons and synapses being well developed. Particularly, electronic synapses based on resistive switching phenomena have been widely studied among different research groups [2]. Moreover, in the extension of more durable, reliable and having specific characteristics devices, e.g. analog-type resistive switching, oxide heterostructures are getting increased attention nowadays [3-4].

In this study, we have investigated multilevel resistive switching (RS) characteristics in low-power and analog-type RS Pt/SiO_x/ZnO/Pt stack oxide heterostructures with scaling down device from 100 μm to 5μm. According to the obtained results, DC and AC electrical characteristics of all devices are closely mimicking biological synapse analog-type behavior, i.e. depending on the number, height and time width of pulses applied to device, current response relaxes to its original state or stays at the different levels.

2. Experiment

Pt/SiO_x/ZnO/Pt oxide heterostructures were fabricated within various device sizes from 100μm to 5μm. Firstly, platinum (Pt) bottom electrode was prepared on pre-cleaned p-Si/SiO_2 substrates by e-beam evaporator. After, using diethyl zinc (DEZ) as a precursor and H_2O as an oxidant, ZnO films were deposited by ALD at 150°C. SiO_x thin films were prepared by RF-sputter, using pure Si (99.99%) target and varying Ar/O_2 ratio to control stoichiometry of the films. Finally, Pt top electrode was prepared by direct sputtering. Same steps were applied for via-hole (5μm) device structure with intermediate steps as next: (PECVD) of SiO_2 on Pt bottom electrode and via-hole etching in standard buffer oxide etchant (BOE) within 45 sec. Thickness of all oxides were defined by ellipsometry. Metal thickness and via-hole depth after etching were measured by α-step. All I-V electrical characterizations were performed on 4200-SCS Keithley semiconductor parameter analyzer at room temperature and atmospheric pressure. Electrical bias was applied on top electrode while bottom electrode was grounded.

3. Results and Discussion

Figure 1 shows schemes of fabricated Pt/SiO_x/ZnO/Pt devices with various dimensions and its optical images. Figure 2 shows I-V characteristics of 100 μm-sized devices. Voltage forming-free and current rectifying (ratio I_F/I_R~14.5) behavior were observed for all devices, while performing resistance switching hysteresis loops. Rectifying behavior is attributed to stacked oxides and metal Schottky contacts. Hysteresis loops are attributed to controlled oxygen stoichiometry in SiO_x and ZnO thin films. Multilevel resistance switching characteristics were observed by applying gradual voltage sweeps during SET regime alike 0.5V→0.75V…1.5V and similar during RESET regime -0.5→-0.75V…-1.2V. Figure 3 shows I-V characteristics of 5μm-sized Pt/SiO_x/ZnO/Pt devices. Resistance switching hysteresis loops appeared from pristine state for all devices, meaning no voltage forming is needed. Rectifying ratio (I_F/I_R~66) and dynamic window of RS hysteresis at SET regime (I_{OFF}/I_{ON}~6.4) and RESET regime (I_{OFF}/I_{ON}~2.7) are improved compare to bigger size devices. Interestingly, the direction of SET/RESET switching regimes changed compare to 100 μm-sized devices, indicating device size dependent RS behavior and effects of filament formation mechanism. No visible degradation of resistive switching was observed during DC cycling. Figure 4 shows multilevel resistance switching I-V characteristics of 5 μm-sized devices. Gradual voltage sweep increase at SET (-1.5V→-1.75V…) change resistant states of device from high resistant state (HRS) to low resistant state (LRS) in monotonic fashion. Same procedure was applied in RESET regime. To obtain higher RS dynamic window devices also have been switched at maximum operating voltages, i.e. -3V at SET and 3.5V at RESET, and effective windows were I_{OFFavg}/I_{ONavg}~5 at SET and I_{OFFavg}/I_{ONavg}~5.5 at RESET, respectively. Figure 5 shows pulse characteristics with varied voltage height and time width applied to 5μm-sized devices. During SET, while read at -0.2V after applied 5μs-width pulses, all devices exhibited current gradual increase and relaxation to its original state, indicating similar to biological short-term memory (STM) synaptic behavior. However, after 50 μs-width pulses applied, similar current characteristics were obtained but with the number of pulses current does not relax fully to its original state, having different current/RS states. Permanent distinguished resistance switching states is similar to biological long-term memory (LTM) synaptic behavior. Figure 6 shows pulse characteristics applied at RESET regime. After, 300 μs-width pulses applied, similarly to SET regime, current relaxation to the distinguished levels/RS states with certain number of pulses was observed, completing device ability to be switched at both SET/RESET regimes gradually like analog-type synapse.

4. Conclusions

A reliable and analog-type multilevel RS behavior from high resistance state (HRS) to low resistance state (LRS) (or vice versa) was observed in Pt/SiO_x/ZnO/Pt 5μm-size devices. Acceptable dynamic window and uniform current distribution in all 50 DC cycles were shown. Synaptic behavior such as STM and LTM were demonstrated by applied pulses and measuring current through device.

Acknowledgements

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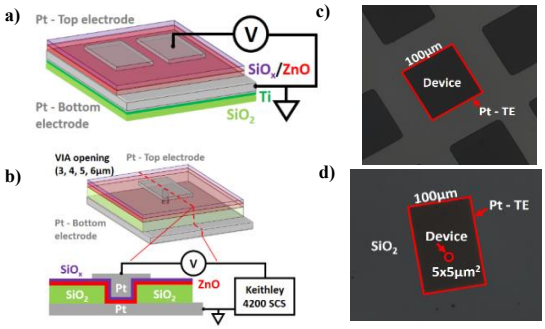

Fig. 1 Schemes of the Pt/SiO_x/ZnO/Pt devices and its optical microscope view

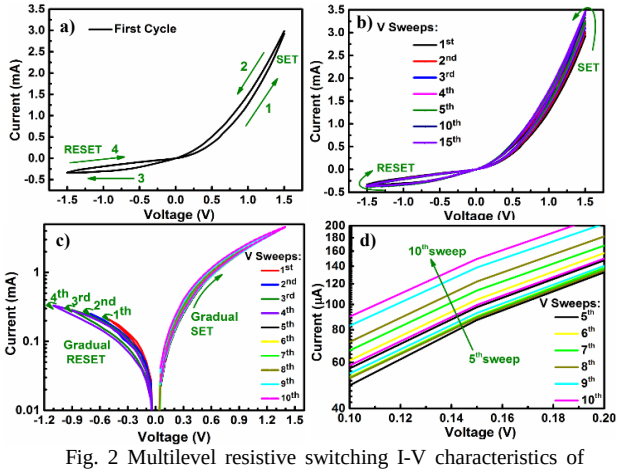

Fig. 2 Multilevel resistive switching I-V characteristics of 100μm-size Pt/SiO_x/ZnO/Pt devices

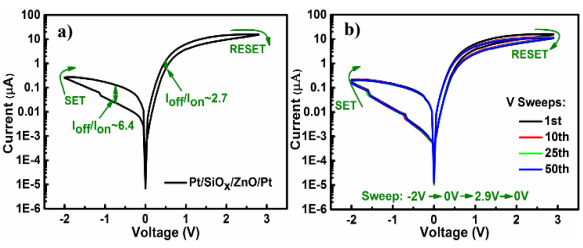

Fig. 3 Resistive switching hysteresis loops I-V characteristics of 5μm-size Pt/SiO_x/ZnO/Pt devices

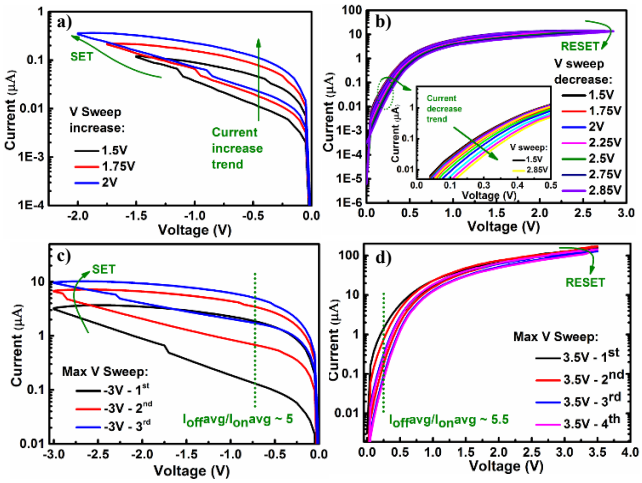

Fig. 4 Multilevel resistive switching I-V characteristics of 5μm-size Pt/SiO_x/ZnO/Pt devices

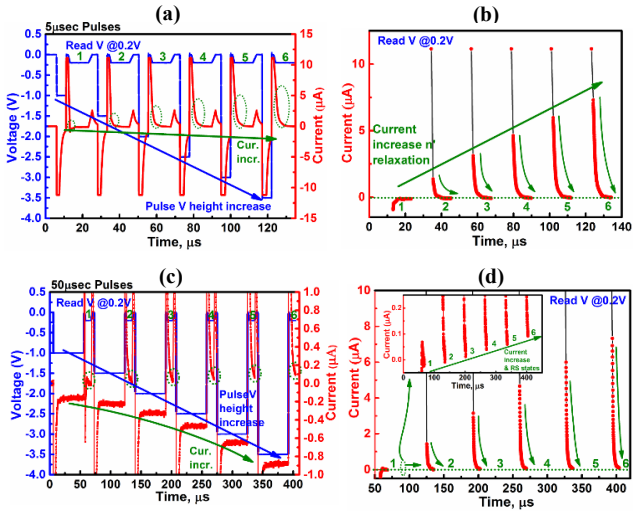

Fig. 5 Pulse measurements of 5μm-size Pt/SiO_x/ZnO/Pt devices in SET regime; Current read at -0.2V.

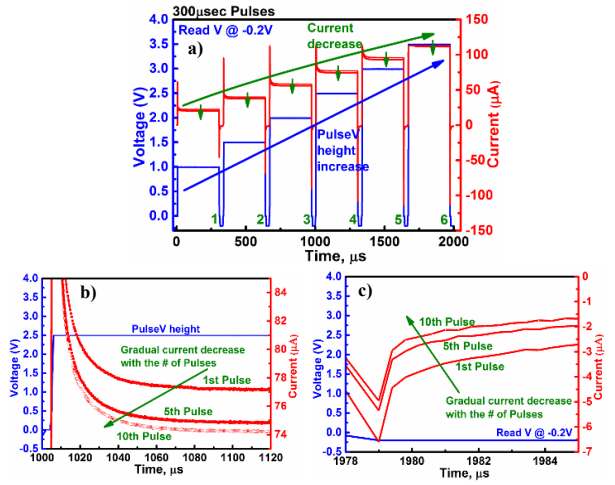

Fig. 6 Pulse measurements of 5μm-size Pt/SiO_x/ZnO/Pt devices in RESET regime; Current read at -0.2V.