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Characterization of Deep Trapping States in Chemical Vapor Deposited Silicon Nitride by Deep Level Transient Spectroscopy

Nao Shinoda and Takuo Kikuchi

Corporate Manufacturing Engineering Center, Toshiba Corporation
33, Shin-Isogo-cho, Isogo-ku, Kanagawa 235-0017, Japan
Phone: + 81-50-3175-6199 E-mail: nao.shinoda@toshiba.co.jp

Abstract

Deep trap levels in a silicon nitride (SiN) film were characterized using a modified deep level transient spectroscopy (DLTS). In order to observe deep trapping states in SiN bulk, electrons were injected into SiN by tunneling current with high electric field across the SiN film and then the capacitance response during emission from these SiN bulk traps was analyzed. By using this method, two levels of electron traps were detected which are known to be attributed to excess Si.

1. Introduction

Silicon nitride (SiN) has been widely used as a gate dielectric for state-of-art transistors in Si microelectronics [1, 2]. However, it has been known that high density traps, which lead to degradation and instability of device properties, are formed both at the SiN-Si interface and in SiN bulk during deposition process [3, 4]. The traps at the interface have been widely studied with various techniques, including Capacitance-Voltage (C-V), Current-Voltage (I-V) measurements and deep level transient spectroscopy (DLTS) [5-8]. However, there have been a few studies which investigate energetically deep levels in SiN bulk [9,10], since use of these techniques above are limited to analysis of traps in semiconductors and at the interface.

This paper proposes a modified DLTS measurement combined with electron injection into SiN film to characterize deep trap levels.

2. Experimental procedure

A metal-insulator-semiconductor (MIS) capacitor was prepared for DLTS measurement. Figure 1(a) and (b) shows structure and process flow of the MIS capacitor respectively. A SiN film with the thickness below 10nm was formed on n-type Si (001) substrate by chemical vapor deposition (CVD). The post deposition annealing was performed above 700°C in N_2 ambient. Au electrode of 100nm in thickness and 1mm^2 was vapor-deposited on the SiN film. The DLTS system (PhysTech Inc.) consists of cryostat (Janis VFP-800), temperature controller (Lakeshore 335), capacitance meter (Boonton 7200) and pulse generator (Agilent 33500B). DLTS measurement was carried out in the constant-capacitance mode as described in details in literature [11, 12]. The sequence of the DLTS measurement and the resulting capacitance change were shown in Fig.2. The initial carrier emission pulse bias, V_r, was kept -1V in the initial phase (1). In the capture phase (2), the carrier injection bias, V_p, was varied from 0, to 2, 4, 10V to control the injection of electrons into the SiN film. The injection pulse width (t_p) for electron capture was 10s long enough to reach an equilibrium of trap filling process. In the emission phase (3), capacitance measurement was extended up to 400s to observe an emission response of deep levels in the SiN film. Capacitance transients were recorded from 320 to 550K to obtain DLTS signals and analyzed using various emission time (t_w) to extract trap energy levels and capture cross sections.

3. Results and Discussion

Figure 3 shows the C-V curve of the MIS capacitor. From the result, the flat band voltage (V_{fb}) was determined to be 0.7V. Figure 4 shows the temperature dependence of the capacitance transient during emission phase (3) in Fig.2 when $V_p = 2V$. This result shows the capacitance increased in time and time constant became shorter with increasing temperature. In order to explain this result, energy bands of the MIS capacitor corresponding to the three phases of Fig.2 are shown in Fig. 5. In the phase (1), the surface of the silicon substrate of the MIS capacitor is kept in depletion (depletion layer width, W_d). When V_p is applied to the gate electrode during the phase (2), the electrons in the accumulation layer tunnel into the SiN and fill the traps, which leads to extension of W_d. In the phase (3), the trapped electrons with an energy above the Fermi Level are emitted at the rate depending exponentially upon temperature. As a result, the extended W_d is reduced to the initial width in the phase (1) and capacitance increases. Therefore the increase of capacitance and shortened time constant suggest electrons were de-trapped during the emission phase.

Figure 6 shows DLTS spectra when applying various V_p. A broad peak at the temperature between 420 and 470K emerged when $V_p \geq 2V$ and the intensity of the peak increased with increasing V_p. The result indicates the peak belongs to the traps in SiN bulk rather than those at the interface and in Si, since the trap levels at the interface and in Si were mostly occupied by electrons when applying V_p higher than V_{fb}. The peak was deconvoluted into two peaks and Arrhenius plots of the two peaks at $V_p = 2V$ are shown in Fig.7. The energy level and the capture cross-section of the two traps were calculated with the least squares method and the results are summarized in Table 1. Two electron traps at 1.66eV and 1.06eV below the conduction band edge were observed. It is considered that each trap level originates from excess Si as Si-Si bond or/and nitrogen vacancy in SiN reported in the literature [3, 13].

4. Conclusion

Characterization of deep level traps in SiN film was performed using DLTS measurement. In order to observe deep levels in SiN bulk, the electron injection into the SiN film through tunneling current was employed. The proposed method successfully detected two levels of electron traps at 1.66V and 1.06eV below the conduction band edge which are known to be attributed to excess Si as Si-Si bond or/and nitrogen vacancy in SiN.

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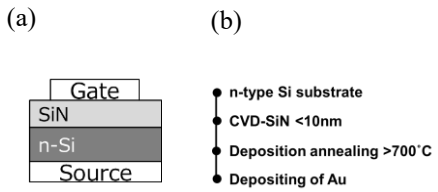

Fig.1 (a) Structure and (b) process flow of the MIS capacitor for DLTS measurement.

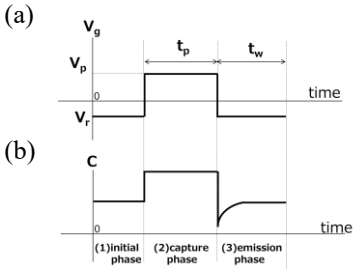

Fig.2 Illustration of (a) sequence of the bias voltage and (b) the capacitance change during DLTS measurement.

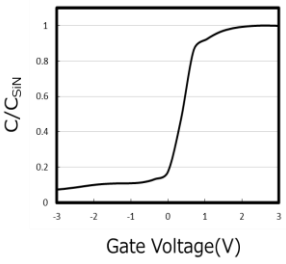

Fig.3 C-V curve of the MIS capacitor.

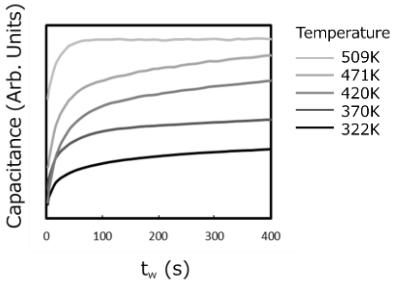

Fig.4 Temperature dependence of the capacitance transient during emission phase (3) in Fig.2 with V_p=2V.

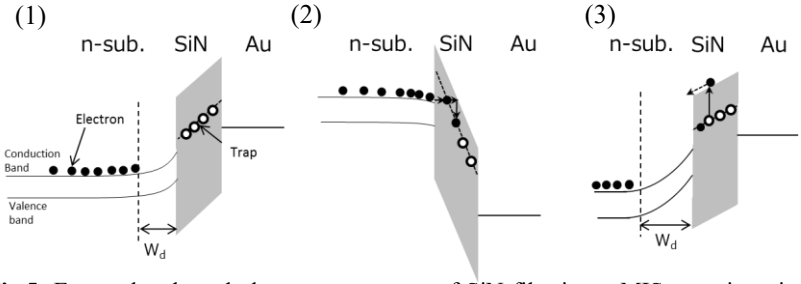

Fig.5 Energy bands and electron occupancy of SiN film in an MIS capacitors in (1) initial phase with a quiescent bias V_r, (2) capture phase with a bias V_p and (3) emission phase with a bias V_r corresponding to Fig.2.

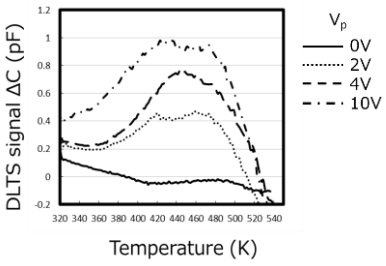

Fig.6 DLTS spectra measured by applying various injection pulse voltage (V_p). The intensity of DLTS signal increases with bias voltage V_p.

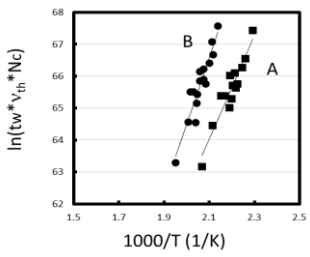

Fig.7 Arrhenius plots of two traps observed in MIS capacitor for the determination of energy levels and capture cross-sections of the traps.

Table 1. Energy levels and capture cross-sections measured by DLTS measurement.

Traps	Energy levels Ec-Et (eV)	Capture cross sections (cm^2)
A	1.058	1.68×10^{-17}
B	1.660	4.67×10^{-12}