

# First Study of High-Ge-Content Si<sub>0.16</sub>Ge<sub>0.84</sub> Gate Stack by Low Pressure Oxidation

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## Abstract

In this study, we employed low pressure oxidation (LPO) to achieve a high quality dielectric gate stack on high-Ge-content (HGC) Si<sub>0.16</sub>Ge<sub>0.84</sub>. We designed a Si-cap free passivation, and the interface trap density ( $D_{it}$ ) was reduced to  $5.1 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$  by optimized process condition. X-ray photoelectron spectra of the interfacial layer (IL) showed that nearly GeO<sub>x</sub>-free IL was detected as 0.01 torr O<sub>2</sub> pressure at 600 °C was used. The gate leakage current in accumulation ( $V_{FB}$ -1V) was also greatly reduced with EOT < 1.5 nm. Finally, the mechanism of LPO oxidation of SiGe is proposed.

## 1. Introduction

HGC SiGe has been considered to be the promising material due to its high hole mobility and superior comparability with conventional Si substrate. However, forming the high quality passivation layer at SiGe surface remains challenges as undesired GeO<sub>x</sub> creates high  $D_{it}$  in the bandgap [1-2]. Low pressure oxidation of SiGe surface is an effective method to suppress the GeO<sub>x</sub> formation due to the difference in Gibb's free energy between SiO<sub>2</sub> and GeO<sub>2</sub> [3] and insufficient O<sub>2</sub> flux to react with the Ge atoms at SiGe surface [4].

In this study, we firstly demonstrate the high quality gate stack formed on HGC SiGe with the help of LPO process. We find that the composition of IL could be effectively controlled by temperature and pressure, and  $D_{it}$  value could be improved by this technique.

## 2. Experiment

Figures 1 (a) and (b) show the detailed process flow and MOSCAP structure. HGC Si<sub>x</sub>Ge<sub>1-x</sub> layer on relaxed Ge buffer layer was grown on low doped p-type Si (100) substrate by LPCVD system. The XRD analysis indicated that the Ge content of SiGe layer was approximately 0.84, as shown in Fig. 1(c). For the fabrication of MOSCAPs, the SiGe wafers were cleaned by diluted HF and DI water to remove native oxides. Then, we used LPO to form the GeO<sub>x</sub>-free interfacial layer (IL), which the oxidation temperature and O<sub>2</sub> pressure were 400/600 °C and 0.3/0.01 torr, respectively. Subsequently, we used Plasma-Enhanced ALD (PE-ALD) to deposit 40 cycles HfO<sub>2</sub> at 250 °C. To improve the quality of gate stack, the post deposition annealing (PDA) in N<sub>2</sub> ambient was used at 300 °C for 1 minute. For the gate electrode, TiN was sputtered and patterned using lift-off process. Finally, Ti/Al was deposited

on the backside of wafer as the body contact. Fig.1 (d) shows the cross-sectional TEM image of the MOSCAP.

## 3. Results and Discussion

First, we investigated the effect of temperature and pressure on Si<sub>0.16</sub>Ge<sub>0.84</sub> surface oxidation. Fig. 2 shows the multi-frequency Capacitance-Voltage (C-V) characteristics of the TiN/HfO<sub>2</sub>/IL/SiGe. The cases of 600 °C with two pressure conditions showed the smaller hump in the depletion and weak inversion regions, and the 600 °C/0.01 torr case depicted the least hump than other cases. Fig. 3 shows the  $D_{it}$  value extracted by conductance method and the MOSCAP gate leakage current with the inset of equivalent oxide thickness (EOT). It revealed that the value of  $D_{it}$  was effectively reduced with higher temperature and lower O<sub>2</sub> pressure. Moreover, the gate leakage current in accumulation ( $V_{FB}$ -1V) of 600 °C/0.01 torr case was around 1 order of magnitude smaller than other cases with a relatively moderate EOT (approximately 1.3 nm).

Next, we examined the XPS spectra of Si2p and Ge3d core levels, as illustrated in Fig. 4. As the temperature increased from 400 to 600 °C, the binding energy of Si-O bonds were increased, indicating that more stable oxide states (Si<sup>3+</sup>, Si<sup>4+</sup>) were formed in the IL. The growth of GeO<sub>x</sub> was effectively suppressed with decreasing O<sub>2</sub> pressure from 1 atm to 0.01 torr. In addition, we extracted the percentage of SiO<sub>x</sub> and GeO<sub>x</sub> in the IL by using the peak area and relative sensitivity factor, as shown in Fig. 5. It suggested that the case of 600 °C/0.01 torr possessed a higher SiO<sub>x</sub> composition with a relatively low GeO<sub>x</sub> formation in the IL, which could result in the reduction of  $D_{it}$  value and significant decrease of gate leakage current. Moreover, the reason of  $V_{FB}$  shift was possibly due to the change of dipole charge and oxide charge, which might be attributed to the increase of Ge concentration at the interface.

Figure 6 shows the speculated schematic illustration of LPO process in the IL formation. During the LPO process, silicon is selectively oxidized leaving behind Ge atoms at the IL/SiGe interface; therefore, if more Si atoms participate in the oxidation reaction, the Ge concentration near the SiGe surface will increase significantly, which evidences that the preferable SiO<sub>x</sub> concentration is controllable by using the LPO.

## 4. Conclusions

We firstly investigate the LPO to improve the properties

of  $\text{Si}_{0.16}\text{Ge}_{0.84}$  gate stack with moderate EOT <1.5 nm and low gate leakage current while it greatly reduces the  $D_{it}$  value ( $5.1 \times 10^{12} \text{ eV}^{-1}\text{cm}^{-2}$ ). The XPS spectra showed that preferable higher  $\text{SiO}_x$  composition with lower  $\text{GeO}_x$  composition in the IL is controllable by using the LPO. The LPO process is a promising approach to be applied on HGC SiGe channel MOSFETs.

### Acknowledgement

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### References

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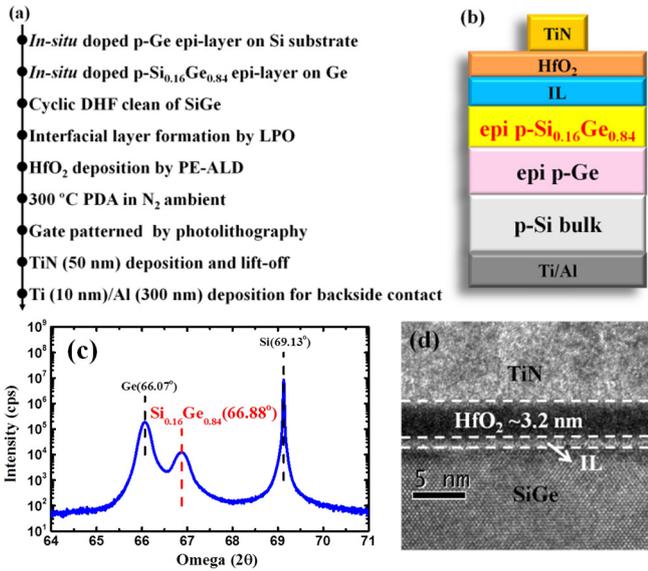


Fig. 1 (a) Process flow and (b) schematic structure of the MOSCAPs. (c) XRD spectra for the HGC  $\text{Si}_x\text{Ge}_{1-x}$  layer grown on relaxed Ge layer. (d) TEM image of the MOSCAP.

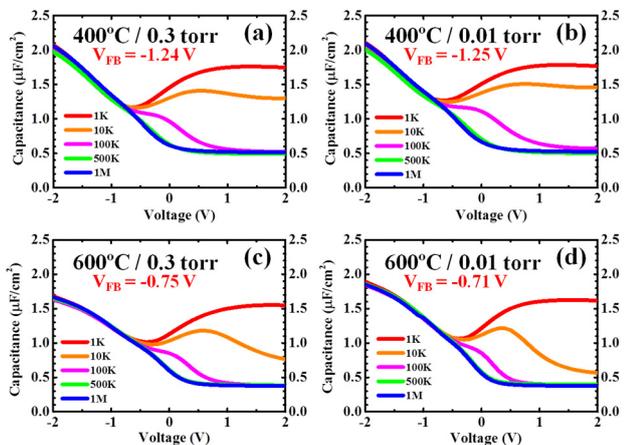


Fig. 2 C-V characteristics of the TiN/ $\text{HfO}_2$ /IL/SiGe MOSCAPs

with conditions of (a) 400 °C/0.3 torr (b) 400 °C/0.01 torr (c) 600 °C/0.3 torr (d) 600 °C/0.01 torr, respectively.

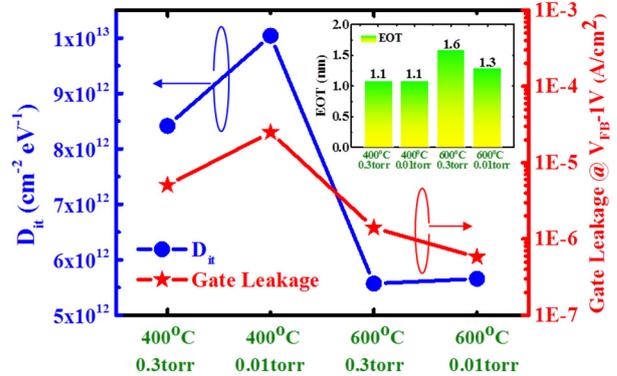


Fig. 3 Comparison of  $D_{it}$  value and gate leakage current. Inset: Corresponding EOT of MOSCAPs extracted by C-V curve.

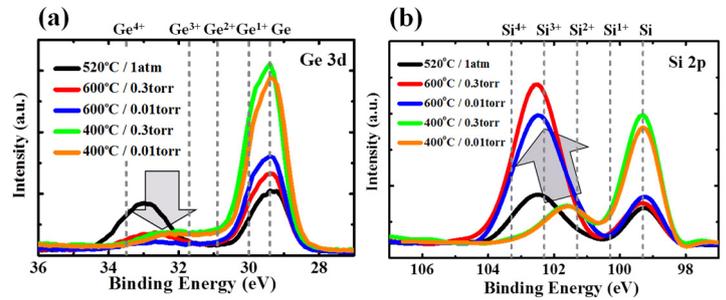


Fig. 4 XPS spectra of (a) Si 2p and (b) Ge 3d of the IL by LPO on SiGe substrate and control sample (520 °C / 1 atm).

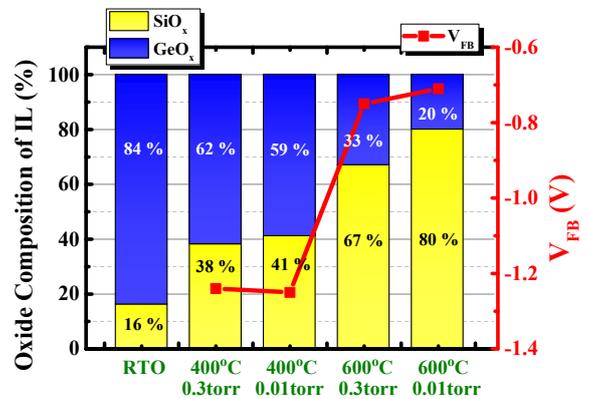


Fig. 5 IL composition on  $\text{Si}_{0.16}\text{Ge}_{0.84}$  determined by XPS curve fitting and  $V_{FB}$  extracted by C-V curve.

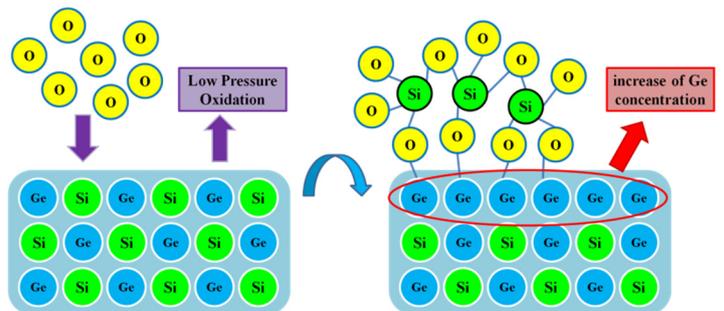


Fig. 6 Illustrative cartoon of the LPO process in the IL formation.