Effect of High Pressure Annealing on the Reliability of FDSOI Tunneling FET

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Abstract

Influences of bulk traps and interfaces traps in the high-k gate dielectric on the reliability of tunneling field effect transistor (tFET) have been investigated by comparing the effect of positive bias temperature instability (PBTI) and hot carrier effect (HCE). During the hot carrier stress, the interface of high-k dielectric and silicon substrate near p/n^+ region was primarily degraded.

High pressure annealing (HPA) in hydrogen is found to be effective in the recovery of high-k dielectric/silicon interface. Also, the variation in the voltage gain of tFET inverter was improved by the HPA.

1. Introduction

Tunneling field effect transistors (tFET) have attracted much attention due to their potential advantages in the extremely low power systems based on the sub-60mV/dec subthreshold swing and the very low off-current. [1]–[3]. In order to improve the performances of tFET, much research in the device structure has been perform by modifying the device structure, introducing new materials, or optimizing the fabrication technology [4]–[6]. However, reliability aspects of tFET has not been studied extensively so far [7]–[9]. In case of tFET, it is expected that the traps near the tunneling injection region can increase swig and degrade the device performances[10]. In this work, the effects of high pressure hydrogen anneal on the reliability of tFET have been investigated by comparing PBTI and HCE.

2. Device Fabrication and Experiment Description

Very thin SOI wafer (t_{si} =50nm) was used as a substrate to make a long channel tFET with channel width and length = 10µm/5µm. As and BF₂ were implanted to form the n-type and p-type junction. Then, 5nm HfAlO_X gate dielectric was deposited using ALD. Finally, TiN gate metal was deposition and patterned using photolithography and etching.

The electrical characteristics of tFETs were analyzed using a semiconductor parameter analyzers (Keithley 4200-SCS). PBTI ($V_G=2V$, $V_D=0V$) and HC stress ($V_G=2V$, $V_D=2V$) were applied for 1000s to evaluate the reliability characteristics of tFETs



Fig. 1 p/n^+ tunneling current and p^+/p tunneling current. 0.7V of drain bias was applied.



Fig. 2 I_D-V_G characteristics before and after 1000s positive bias (a) and hot carrier stress (b). Gate voltage shifts ΔV_G at the same drain current I_D after the positive bias (c) and hot carrier stress (d), as function of I_D.

3. Result and Discussion

Fig. 1 shows the typical transfer curve (I_D-V_G) of tFET and the band diagram showing the tunneling currents with/without a gate bias. There is an initial band bending due to the drain bias, which generates the high leakage current at p/n^+ junction. As the V_G increases, p/n^+ tunneling current decreases and p^+/p tunneling current increases. It is the typical ambipolar characteristics of tFETs.

Fig. 2 (a) and (b) shows the typical I_D -V_G curves before and after PBTI and HCE stress. After PBTI stress, the I_D -V_G curves shifted in parallel (Fig. 2(a)), indicating that the charge accumulation at the bulk trap sites. The direction of I-V curves indicates primary charging carriers are electrons. Fig. 2 (c) shows that the amount of charge traps measured by ΔV_G is not influenced by the drain current level.

On the other hand, after the HC stress, the slope of both p/n^+ and p^+/p tunneling current region of I_D -V_G curve decreased as shown in Fig. 2(b). The slope change in the p/n^+ tunneling current region appears to be more pronounced. The decrease of slope is proportional to the transconductance (g_m) and g_m decrease can be considered as a reduction of mobility due to the increased scattering by the interface traps. Interface trap generation near the drain site is a typical phenomenon for silicon MOSFET because of the strong electric field after the pinch off point. Since the major difference between tFET and silicon MOSFET is in the injection point, it may be natural to see the interface trap generation near the drain site of point.

In order to investigate the role of various traps in tFET operation, I_D -V_G curves were measured at 220K and 330K as shown in Fig.3(a), and the shift in the I-V curves monitored before and after the HPA to measure the relative changes p/n⁺ and p⁺/p tunneling current.



Fig. 3 (a) Temperature dependence of I_D -V_G characteristics. Gate voltage shifts ΔV_G by temperature at the same drain current I_D . (b) Device scheme and expected interface trap position generated by hot carrier stress. (c) Temperature dependence of p/n^+ tunneling current before, after stress and after HPA. (d) Temperature dependence of p^+/p tunneling current before, after stress and after HPA.



Fig. 4 (a) Temperature dependence of tFET inverter. (b) Voltage gain variation before and after HPA.

Fig. 3 (c) and (d) show the temperature dependency of p/n^+ and p^+/p tunneling current region. In both cases, the temperature dependence of tunneling current increased after the HC stress, indicating the enhanced trap generation by the HC stress at elevated temperature. The increase was slightly higher at p/n^+ tunneling current region than p^+/p tunneling current region. This result matches with the slope change shown in Fig. 2(b). On the other hand, the temperature dependency significantly decreased after the HPA at both p/n^+ and p^+/p tunneling current region. This result indicates that the hot carrier stress in tFET is also related to Si-H bonds.

Fig. 4 (a) shows the temperature dependence of tFET inverter. The variation of voltage gain is substantially reduced after HPA. These results confirm that the high pressure hydrogen anneal is a very crucial process to stabilize the operation of tFET.

3. Conclusions

In this study, we have shown that the reliability of tFET and inverter can be enhanced by through high pressure hydrogen annealing. Both PBTI and HCE were substantially improved. As a result, the variation in the voltage gain of tFET based inverter was substantially reduced.

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References

- [1] A. M. Ionescu and H. Riel, Nature, 479 (2011) 329.
- [2] H. Lu and A. Seabaugh, IEEE J. Electron Devices Soc., 2, (2014) 44.
- [3] W. Y. Choi et al., IEEE Electron Device Lett., 28 (2007) 743.
- [4] M. Kim et al., IEEE Trans. Electron Devices, 62 (2015) 9.
- [5] G. B. Beneventi et al., IEEE Trans. Electron Devices, 613 (2014) 776.
- [6] R. Gandhi et al., IEEE Electron Device Lett., 32 (2011) 437.
- [7] A. Vandooren et al., IEEE Trans. Electron Devices, 61 (2014) 359.
- [8] G. F. Jiao et al., IEEE International Electron Devices Meeting (IEDM) (2009) 1.
- [9] X. Y. Huang et al., IEEE Electron Device Lett., 31 (2010) 779.
- [10] L. Ding et al., IEEE Trans. Device Mater. Reliab., 15 (2015) 236.