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INVESTIGATION OF LONG TERM ELECTRICAL TRANSPORT STABILITY OF MoS_2 FLAKES

Hüseyin Şar[1], Ayberk Özden[2], Cem Odacı [1], Cem Sevik[3], Nihan Kosku Perkgöz[1], Feridun Ay[1]

[1] Anadolu Univ.
Department of Electrical and Electronics Engineering, Faculty of Engineering, 26555, Eskisehir, Turkey
Phone: +90-222-335-05-80, E-mail:hsar@anadolu.edu.tr
[2] Anadolu Univ.
Department of Materials Science and Engineering, Faculty of Engineering, 26555, Eskisehir, Turkey,
[3] Anadolu Univ.
Department of Mechanical Engineering, Faculty of Engineering, 26555, Eskisehir, Turkey

Abstract

The electrical stability of the cracked and crack-free MoS_2 flakes which are grown with two different approaches by CVD are investigated in terms of electrical transport properties. Flakes grown by Face Down CVD method are observed to spontaneously develop cracks with time. On the other hand, flakes grown by horizontal CVD approach remains intact and crack-free (for this research, this duration is limited by a period of 18 months). Although the FD grown flakes are cracked, the fabricated devices from these flakes are still functioning. FET performance of the MoS_2 flakes, grown by two different, face-down and horizontal methods using CVD are realized and compared.

1. Introduction

Low dimensional materials such as graphene, monolayer or few layer MoS_2, WS_2 are promising candidates for future electronic and optoelectronic applications because of their unique properties such as very high carrier mobility, high current on/off ratio, very high quantum yield and extreme mechanical properties [1]. Not only their single-layered devices, but also their heterostructures present high potential for various applications [2]. Among 2-D materials, MoS_2 attracts considerable attention for electronic and optoelectronic applications, due to its wide band gap (1.3 – 1.8 eV) range [3], high current on/off ratio and large scale production potential by using chemical vapor deposition (CVD). Considerable amount of research has been conducted on the physical and structural properties and basic device characteristics of the CVD grown MoS_2 [4]. However, there are limited studies on the structural stability of the monolayer MoS_2 and its FET characteristics [5-7]. Understanding the life span of MoS_2 and MoS_2 based devices is critical and still an open problem in terms of long-term structural and device stability. Cracking and aging problem of MoS_2 are referred to the residual thermal strain effect (induced during growth) and oxidation (environmental effects) [5-7]. However, it is still not enough to elucidate the reliability of MoS_2 devices from the point of long term mechanical integrity and electronic performance. Hence, in this work, the FET performance of the MoS_2 flakes, which are grown by two different, face-down and horizontal methods using CVD are demonstrated and compared. The device fabrication and analysis are performed on the 18 months old flakes, which possess unique structural differences depending on the growth conditions.

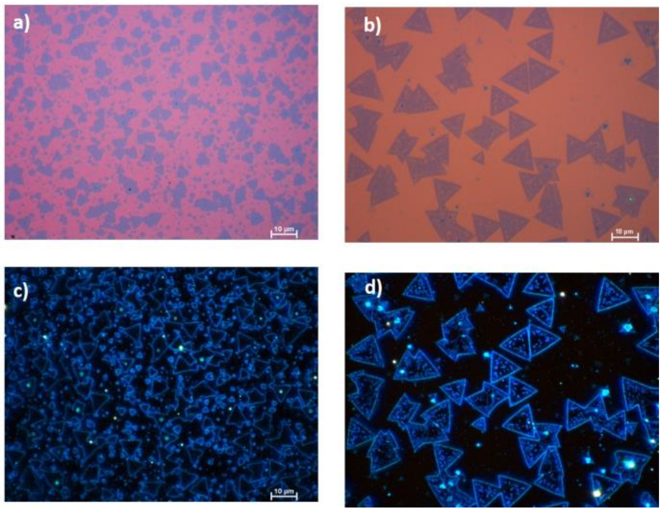

Fig 1. Bright and dark-field microscope images of H (a and c) and FD (b and d) grown MoS_2 flakes.

2. Experimental Procedure

The MoS_2 flakes are grown by face-down (FD) and horizontal (H) approach. In FD growth, Si/SiO_2 substrates are positioned on top of the MoO_3 precursor and in H growth substrates are positioned next to the precursor. MoS_2 flakes are kept in laboratory environment with no vacuum and thermal process for 18 months. The devices are fabricated on as-grown substrate without any transfer process to eliminate the transfer originated effects. Source and drain electrodes are first patterned by optical lithography and 95 nm Au on top of 5 nm Ti is deposited by thermal evaporation. . N-doped silicon wafer (1-10 Ω.cm) with 270 nm ±35 nm SiO_2 dielectric layer is used as back gate electrode and gate dielectric.

The flakes are characterized by measuring μ-Raman and photoluminescence (PL) spectra. Electrical characterizations are carried out with a home-built probe station.

3. Results & Discussion

Fig. 1 represents the MoS_2 flakes grown 18 months ago by using the two approaches in CVD as mentioned before. Optical microscope image and dark field optical image of H grown flakes indicate continuous triangle without any structural difference after 18 months(Fig 1.a and Fig 1.c). On the other, the flakes in Fig 1.b demonstrate crack like discontinuous regions on the triangles, which can also be visualized in dark field optical image of the same flakes (Fig 1.d) may indicate new edges.

Fig 2.a presents PL spectra of MoS_2 flakes in the channel of the device after the fabrication process. PL spectra of the freshly grown MoS_2 flakes show a high I_A/I_B intensity ratio where I_A is the maximum intensity of A exciton and I_B is the maximum intensity of B exciton. However, after wet processes (fabrication) the PL intensity is seen to decrease because contamination [8]. Fig 2.c shows Raman peak shift of monolayer MoS_2 flakes with a difference of 18 cm^{-1} between E^1_{2g} and A_{1g}, which is typical for monolayer MoS_2. The integrated PL intensity maps of MoS_2 flakes inside the device channels confirm the continuity of the flakes even for those with cracks for FD grown ones (Fig 2.b) and non-grown areas for H grown ones (Fig 2.c).

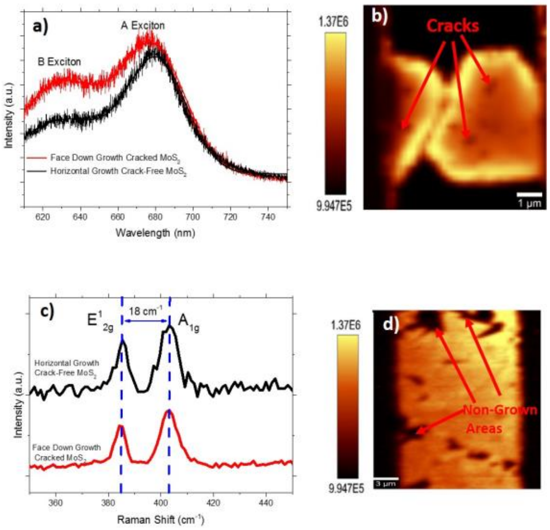

Fig 2. a) Single PL spectrum of cracked MoS_2 in the device channel, b) PL map of cracked MoS2 in the device channel, c) Single Raman spectrums of cracked and crack-free MoS_2 in the device channel and d) PL map of crack-free MoS_2 in the device Channel.

All the fabricated devices are characterized under dark and illuminated conditions. Fig 3.a demonstrates the gating responses of the devices fabricated from crack-free H grown and cracked FD grown flakes. The carrier mobility of cracked and crack-free devices are calculated as 0.08 $cm^2V^{-1}s^{-1}$ and $2.5x10^{-4}$ $cm^2V^{-1}s^{-1}$, respectively. The gating performance of both devices is weak in terms of mobility which is due to thick gate dielectric layer with a low dielectric constant (ε_{SiO2}=3.9). The mobility of devices is found to be very low. The mobility can be improved by the deposition of a high-κ dielectric environment [9]. Another reason of low mobility could be the ambient storage environment of the MoS_2 samples. On the other hand, the cracked device shows a better transfer performance than the crack-free one. Fig 3.b and Fig 3.c. demonstrate the dark and illuminated condition transfer curves. The ratio of the current under illumination over dark current (I_{PH}/I_{Dark}) used as another performance criteria for device comparison. The crack-free device show a better performance than cracked one according to I_{PH}/I_{Dark} ratio. The I_{PH}/I_{Dark} ratio for cracked and crack-free devices are 20.08 and 72.24, respectively.

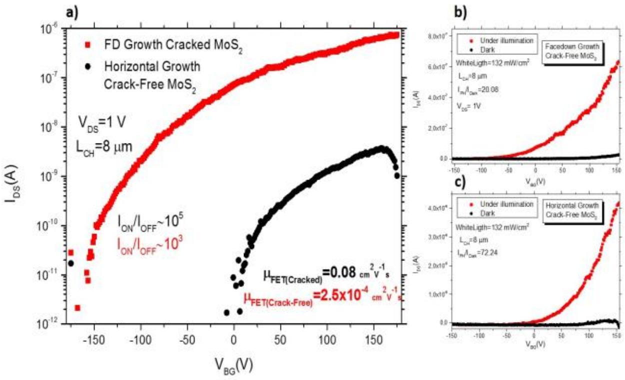

Fig 3. Transfer curve (I_{ds}-V_{BG}) of cracked FD grown and crack-free H grown MoS_2 (a), Gating response of cracked device(b) and crack-free device (c) under dark and illuminated conditions.

4. Conclusions

As a conclusion, the μ-Raman, photoluminescence (PL) spectroscopy analysis and FET performance of MoS_2 flakes grown with two different approaches using CVD and aged about 18 months are demonstrated. The phototransistor performance of the fabricated devices is also investigated. While the cracked devices show better performance as FET, the crack-free device is better as a phototransistor.

Acknowledgements

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