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AC Hot carrier effect and PBTI of a thin-film SOI Power n-MOSFET at high temperature

Masanari Nomura, Akihiko Watanabe, and Satoshi Matsumoto

Kyushu Institute of Technology,
Sensui-cho, Tobata-ku, Kitakyushu-shi, Fukuoka, 804-8550, JAPAN
Phone/Fax:+81-93-884-3234, e-mail:nomura.masanari315@mail.kyutech.jp

Abstract

This paper investigated hot carrier effect and PBTI under AC stress for a n-channel thin-film SOI power MOSFET in high temperature. Degradation rate of on-resistance and threshold voltage shift decrease with increasing temperature.

1. Introduction

High temperature applications of the power devices and power ICs attract attention because of increasing the demand of electric car, jet engine for aircraft, nuclear power plants, and artificial satellite. If the conventional Si technology is applied at high temperature, it fails due to excess leakage current and latch-up.

Silicon on insulator (SOI) technology is one of the promising candidates for it and the thin-film approach is quite promising because it can reduce leakage current and suppress the latch-up [1].

We previously reported the device characters and hot carrier effect and PBTI(Positive Bias Temperature Instability) of the thin-film SOI power MOSFET at high temperature[2,3]. Actually, the AC hot carrier effect is important and we also previously reported AC hot carrier effect at room temperature [4].

In this paper, we explore the temperature dependence of the AC hot carrier effect and PBTI of thin-film SOI nMOSFET.

2. Device structure and Fabrication process

The schematic cross section of the thin-SOI power nMOSFET is shown in Fig. 1. The body contacts were formed to suppress the parasitic bipolar effect.

The main structural parameters are listed in Table 1. The thin-film SOI power MOSFET was fabricated using the 0.5 µm-rule poly-Si gate process with local oxidation of silicon (LOCOS) isolation. The device characteristics are listed in Table 2.

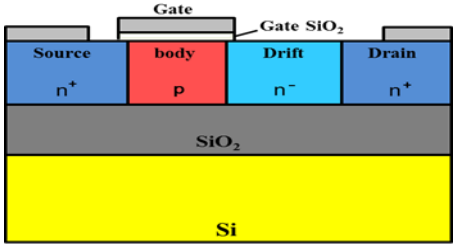

Fig. 1 Schematic cross section of the thin-film SOI nMOSFET.

Table. 1 The main structural parameter.

The name of parameter	Parameter
Gate Oxide (nm)	11
Drift Length (µm)	0.5
Channel Length (µm)	0.5
Top Si layer (µm)	0.14
Buried oxide (µm)	0.4
Gate Width (µm)	20

Table. 2 The device characteristics.

Temperature (K)	300	373	473	573
Channel Length (µm)	0.5			
On-Resistance (Ω·mm)	352	434	595	791
Threshold Voltage (V)*	572	493	394	280
Break Down Voltage (V)**	14.6	14.4	12.5	7.6

*Vg=4.5(V) **Vg=0(V)

3. Results & Discussion

Table 3 shows the mapping of the device destruction or not during stress. Stress time is 3600 seconds, and stress drain voltage is 6V. We use square wave (0V-4.5V) at AC stress. The power MOSFETs do not show destructive failure under DC stress. The device destruction occurs when the switching frequency of 1 kHz and 10 kHz at temperature of less than 473 K. The power MOSETs do not break when the frequency is more than 100 kHz at temperature of less than 473 K. These are caused by accumulation of a minority carrier and this enhances the parasitic bipolar effect [4]. The destruction occurs even at 100 kHz when temperature is 573 K because leakage current at off state become larger at 573 K and this enhances the parasitic bipolar effect.

Dependence of degradation rate of on-resistance on

Table. 3 The mapping of the device destruction or not during stress.

Temperature (K)	Frequency (kHz)					
	DC	1	10	100	1000	10000
300	○	×	×	○	○	○
373	○	×	×	○	○	○
473	○	×	×	○	○	○
573	○	×	×	×	○	○

○...success ×...destruction

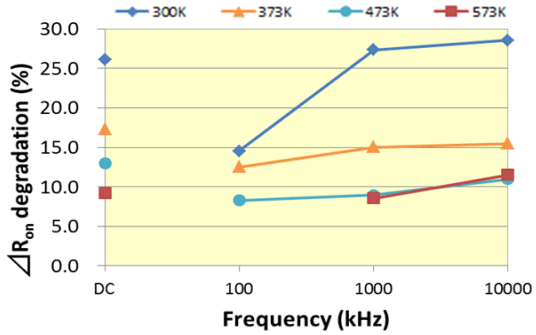

Fig. 2 Dependence of on-resistance on frequency.

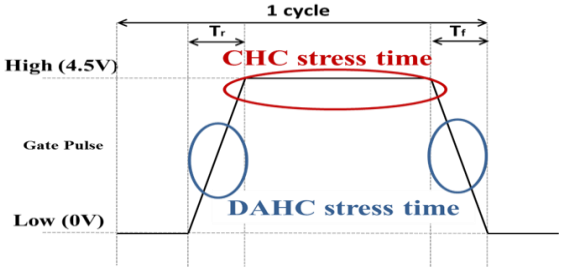

Fig. 3 Gate stress wave form (T_r and T_f = 5n sec).

frequency is shown in Fig. 2.

The gate stress wave form including DAHC(Drain avalanche hot carrier injection) stress time and CHC(channel hot carrier injection) stress time is shown in Fig. 3. DAHC occurs during the rise time and fall time as shown in Fig. 3. CHC injection occurs during high gate voltage (Vg=4.5V). Degradation rate of the on-resistance increases as frequency increases because DAHC time increases as frequency increases. The degradation rate of on-resistance decreases with increasing temperature because impact ionization rate decreases as temperature increases. The degradation rate of on-resistance at 573 K is almost the same at 473 K.

Dependence of threshold voltage shift on frequency is shown in Fig. 4. The threshold voltage shift decreases with increasing switching frequency except for 100 kHz at 300K. The threshold voltage shift also decreases with increasing temperature except for 300 K because of high temperature annealing effect. The threshold voltage shift in DC is larger than in AC.

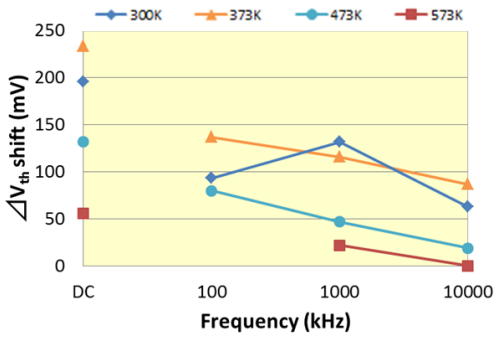

Fig. 4 Dependence of threshold voltage shift on frequency.

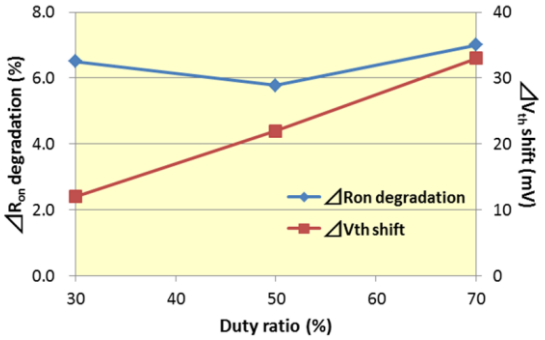

Fig. 5 Dependence of degradation rate of on-resistance and threshold voltage shift on duty ratio at 573K.

Dependence of degradation rate of on-resistance and threshold voltage shift on duty ratio at 573K is shown in Fig.5. The switching frequency is 100 kHz. In this case, total on time (total period during gate voltage of 4.5V) is the same. This means that the stress time changes according to the duty ratio; for example, stress time at duty ratio of 30% is 2006.7 sec. and one at duty ratio of 50% is 1202.4 sec. The degradation rate of on-resistance is almost constant regardless of duty ratio, because the degradation rate of on-resistance saturates at high temperature as shown in Fig. 3. The threshold voltage shift decreases with reducing duty ratio even at the total constant on time. At 573K, threshold voltage shift is caused by PBTI[3] and this recovers during off time. Recovering rate increases as duty ratio reduces and this makes threshold voltage shift small.

4. Conclusions

We clarify the AC hot carrier effect and PBTI of the thin-film SOI power n-MOSFET at high temperature. Degradation rate and the threshold voltage shift reduce as temperature increases. Degradation rate of on-resistance increases and threshold voltage shift decreases with increasing switching frequency.

References

[1] J. P. Colinge, Silicon-on-Insulator Technology: Materials to VLSI (Kluwer Academic, Dordrecht, 2004) 3rd ed., p. 4.

[2] Y. Morisawa, T. Kodama, and S. Matsumoto, J. Microelectronics Reliability, vol.52, pp. 2380-2384, 2012.

[3] W. Yoshida, T. Takasugi, and S. Matsumoto, Jpn. J. Applied Physics, vol.54, No.4S, 04DP17, 2015.

[4] D.Takenaka and S.Matsumoto; Jpn. J. Applied Physics, Vol.56, No.4S, 04CR17, 2017.