

Highly Efficient and Compact CMOS DC-DC Converter with Novel Transistor Layout of 60 nm Multi-pillar Type Vertical Body Channel MOSFET

Kazuki Itoh^{1,2,3,4} and Tetsuo Endoh^{1,2,3,4}

¹Graduate School of Engineering, Tohoku Univ. Japan, ²Center for Innovative Integrated Electronic Systems, ³JST-ACCEL, ⁴JST-OPERA
Phone: +81-22-795-4906 E-mail: tetsuo.endoh@cies.tohoku.ac.jp

Abstract

A novel transistor layout of multi-pillar Vertical Body Channel (BC) MOSFET is proposed and evaluated to achieve highly efficient and compact CMOS DC-DC converters. It shares drain and source of Vertical BC MOSFETs connected in series, therefore the effects of parasitic components on the source and drain are suppressed. Moreover, 2.0 V / 0.8 V 100 MHz CMOS DC-DC converters with the proposed layout with 60 nm Vertical BC MOSFET are designed and simulated by HSPICE. They obtained peak efficiencies of 89.0% with high-side PMOS and 90.1% with high-side NMOS power switch which are 5.4% and 6.0% higher than that with the conventional layout, respectively.

1. Introduction

The Vertical Body Channel (BC) MOSFET shown in Fig. 1(a) is an almost desirable semiconductor device for future digital CMOS because it provides excellent current drivability, scalability and back bias free characteristic [1]. It arranges the source, channel and drain vertically.

In recent logic and memory applications, a CMOS DC-DC converter integrated on the same die such as an integrated voltage regulator becomes a key feature to achieve low-operating-power [2]. The CMOS DC-DC converter with cascode power switches can handle higher voltage than CMOS process voltage with high switching frequency such as 100 MHz; hence the highly efficient cascode MOSFET with Vertical BC MOSFET shown in Fig. 1(b) is demanded.

The layouts of non-cascode multi-pillar Vertical BC MOSFETs with low drain/source parasitic resistances were investigated in the previous work [3]. However, a design methodology of the cascode power switch with multi-pillar Vertical BC MOSFET has not been reported until yet.

In this paper, a novel layout of multi-pillar Vertical BC MOSFET is proposed for CMOS DC-DC converters.

2. Proposed Layout of Multipillar Vertical BC MOSFET

The top view of the proposed transistor layout of the multi-pillar Vertical BC MOSFET is shown in Fig. 2. The proposed layout is composed of two MOSFETs connected in series to assume the cascode power switch. "S" and "D" indicate top node as source with bottom node as drain, and top node as drain and bottom node as source, respectively. The metal and gate layer have a Stacked and Multi-Fingered (SMF) structure. Applying the proposed transistor layout, resistances of bottom contacts and the diffusion layer between the source of M1 and the drain of M2 can be suppressed, because they are shared on the diffusion layer.

The parasitic resistance dependence of series resistance across the drain of M1 and the source of M2 of various transistor layouts are simulated with the method described in the previous work [3]. In conventional layouts, there are 4 in-

termediate bottom contacts in 21 and 26 Si pillars; namely, *inter_21* and *inter_26* as shown in Fig. 3 (a) and (b), respectively. The proposed layouts have 56 Si pillars without a bottom contact. The pillar-to-pillar connections are vertical and diagonal: namely, *SMF_56* and *DSMF_56* as shown in Fig. 3 (c) and (d). The both pillar-to-pillar spacing and pillar diameter is assumed as the feature size F. The area of bottom contact is F×F. The diffusion resistance R_{diff} and contact resistance R_{co} dependence of the series resistance is shown in Fig. 4 and Fig. 5, respectively. Contact resistances are added to both top and bottom of Si pillars. The series resistance is suppressed with the proposed *SMF_56* compared with conventional *inter_26* by 57% for PMOS with $R_{diff}=400\ \Omega$ and 73% for NMOS with $R_{diff}=200\ \Omega$. In the proposed *SMF_56*, the series resistance increase due to the contact resistance is suppressed since the bottom contacts between the source of M1 and drain of M2 are removed.

3. Results of CMOS DC-DC Converter and its Benchmarking

2.0 V / 0.8 V 100 MHz CMOS DC-DC converters composed of cascode power switches with Vertical BC MOSFET are designed and simulated. The both topologies of High-Side PMOS (HSP) and NMOS (HSN) power switch shown in Fig. 6 [4] are simulated. The gate widths of M1-M4 are optimized to obtain the highest efficiency at 0.5 A load current by a numerical analysis. Parameters of the simulated converters are summarized in Table I. The applied MOSFET model is extracted from the experimental data of Vertical BC MOSFET with the 60 nm diameter and 100 nm gate length [5]. Fig. 7 shows the efficiency curves of the converters with the proposed structure compared with the conventional *inter_21*. The converters with the proposed *SMF_56* have 89.0% and 90.1% peak efficiencies with HSP and HSN which are 5.4% and 6.0% higher than that with the conventional *inter_21*, respectively. The benchmarking table of the simulated converters is summarized in Table II. It is worth noting that not only the efficiency is enhanced, but also the area is reduced owing to the shared S/D.

4. Conclusions

A novel transistor layout of multi-pillar Vertical BC MOSFET is proposed to suppress the series resistance of the cascode power switch. From the results, the CMOS DC-DC converters with the proposed layouts with 60 nm Vertical BC MOSFET obtained peak efficiencies of 89.0% and 90.1% for HSP and HSN respectively, which indicates the proposed multi-pillar Vertical BC MOSFET is a promising candidate for the highly efficient and compact CMOS DC-DC converter.

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References

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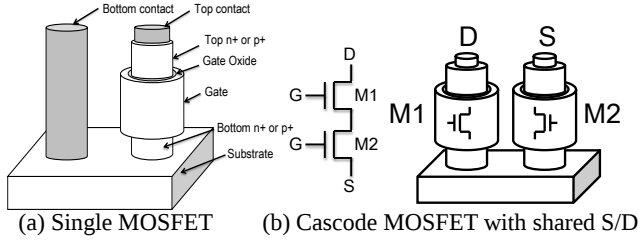


Fig. 1 Bird's eye view of the Vertical Body Channel (BC) MOSFET.

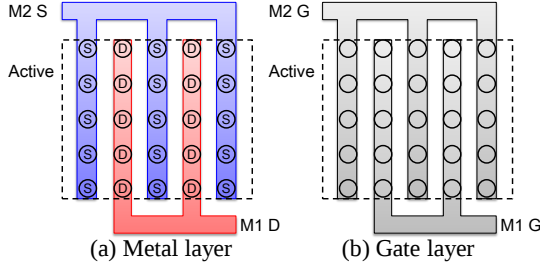
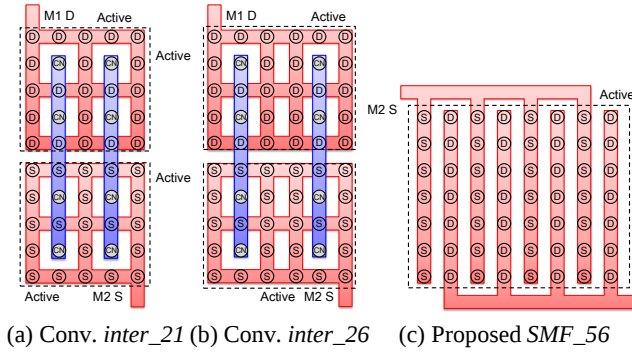
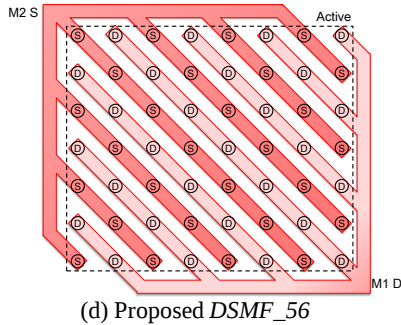


Fig. 2 Proposed layout of the multi-pillar Vertical BC MOSFET.



(a) Conv. inter_21 (b) Conv. inter_26 (c) Proposed SMF_56



(d) Proposed DSMF_56

Fig. 3 The layouts of multi-pillar Vertical BC MOSFETs for CMOS DC-DC converter applications.

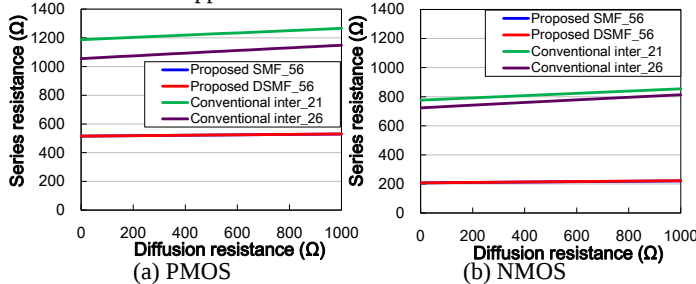


Fig. 4 Diffusion resistance dependence of the series resistance of M1-M2 with the proposed and conventional layouts.

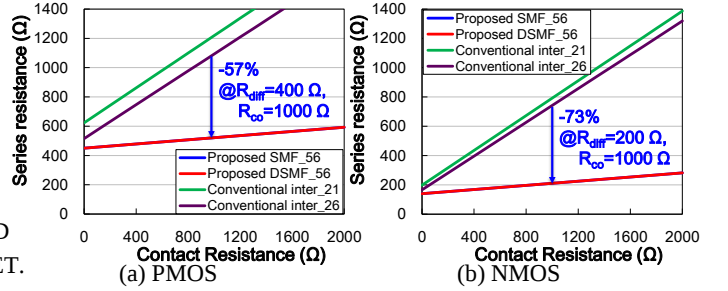


Fig. 5 Contact resistance dependence of the series resistance of M1-M2 with the proposed and conventional layouts.

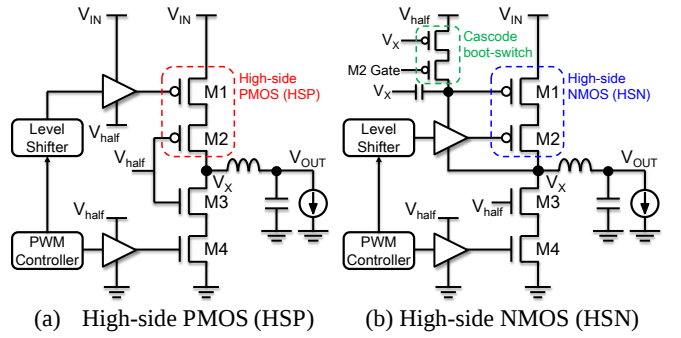
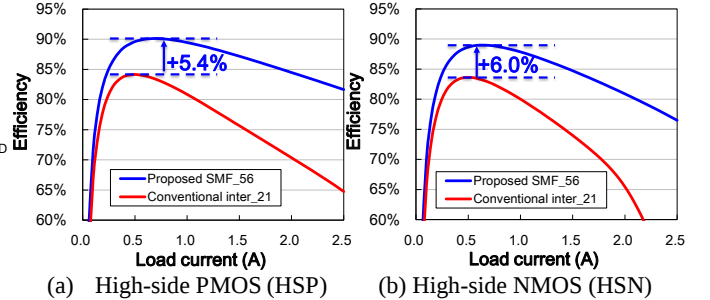


Fig. 6 Schematic of the cascode CMOS DC-DC converters [4].



(a) High-side PMOS (HSP) (b) High-side NMOS (HSN)

Fig. 7 Efficiency curves of the CMOS DC-DC converters with the multi-pillar Vertical BC MOSFET with $R_{diff}=200\Omega$ and $R_{co}=1k\Omega$.

Table I Parameters of the simulated CMOS DC-DC converters.

Input voltage V_{IN}	2.0 V
Half-rail voltage V_{half}	1.0 V
Output voltage V_{OUT}	0.8 V
Inductance	4 nH
Output capacitance	10 μ F
Bootstrap capacitance (High-side NMOS only)	400 pF
Crossover frequency	10 MHz
Switching frequency	100 MHz
MOSFET model	BSIM4 60 nm Vertical BC MOSFET model extracted from experimental data.

Table II Benchmarking table of the CMOS DC-DC converters.

Converter topology	HSP (See Fig. 6 (a))		HSN (See Fig. 6 (b))	
Layout of Vertical BC MOSFET	Proposed SMF_56	Conventional inter_21	Proposed SMF_56	Conventional inter_21
Total area of M1-M4 at optimum gate width (F^2)	2,376,120	2,828,715	1,901,200	2,263,333
Peak efficiency	89.0%	83.6%	90.1%	84.2%
Heavy load efficiency at 2.0 A	80.9%	65.5%	84.5%	70.4%