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Normally-off MOSFET Properties Fabricated on Mg Implanted GaN Layers

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Abstract

In this paper, we present normally-off operation of GaN MOSFETs with the threshold voltage of ~ 10 V on Mg 1×10^{18} cm^{-3} implanted layers. The fabricated MOSFETs show higher field effect mobility with higher temperature annealing for implanted Mg activation. We obtained the maximum field effect mobility of 48.9 cm^2/Vs on the 1400°C annealed surface. These results greatly support GaN for the vertical power switching application.

1. Introduction

Gallium nitride (GaN) is attracting much attention due to its promising material properties for next generation power conversion systems such as the wide bandgap energy and the large critical electric field [1]. For high voltage and large current application, the vertical device structures on GaN bulk substrates (GaN on GaN) are more favorable and the vertical GaN transistors with the breakdown voltages higher than 1 kV have been demonstrated so far [2-4]. However, there are many key issues which have not yet been established for the realization of high performance and reliable vertical GaN on GaN devices.

The demonstrated GaN vertical power transistors utilize the pn junction formed by epitaxially-grown Mg doped layers. As a principle demonstration, we have reported the lateral MOSFETs with controlled threshold voltage (V_{th}) by Mg doping and high channel mobility on epitaxially-grown p-GaN layers [5]. In the actual device fabrication, the impurity doping into the selective area by ion implantation (I/I) is essential technique in order to fabricate a fine device structure of active region for low R_{on} device as well as an edge termination structure such as guard ring or junction termination extension. It is known that the activation of implanted Mg is difficult, but some previous works have reported the possibility of p-GaN formation by Mg I/I [6-9]. However, there is few research for MOS channel properties on it. In this study, we fabricate lateral MOSFETs on Mg implanted GaN layers with different activation annealing conditions, and investigate the MOS channel properties as a key element for a vertical power MOSFET.

2. Device fabrication

Fig. 1 shows a schematic cross section of the fabricated lateral GaN MOSFETs by all-implantation process. Firstly, the Mg I/I was carried out on 4-μm-thick undoped GaN layers grown by using metal organic chemical vapor deposition (MOCVD) on the n-type GaN (0001) substrates obtained by hydride vapor phase epitaxy (HVPE). The threading dislocation density was lower than 10^7 cm^{-2}. The Mg-ions were implanted with 20 to 430 keV to create 500-nm-deep BOX profile with Mg concentration [Mg] of 1×10^{18} cm^{-3}. After Mg I/I, the wafers were annealed at 1200, 1300, and 1400°C with AlN encapsulation cap to prevent dissociation of GaN during high temperature annealing. After the annealing, the AlN cap was chemically removed.

Secondly, Si ions were implanted into the source and drain regions selectively followed by 1100°C annealing for Si activation. After the activation annealing, 110-nm-thick SiO_2 layers were deposited at 300°C by using a plasma-CVD apparatus with TEOS gas. In order to simplify the fabrication process, aluminum metal was used for all electrodes, a gate metal, source and drain contact metal, and also a body contact metal. Finally, we performed a forming gas annealing.

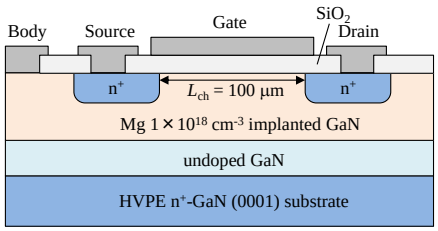

Fig. 1 Schematic cross section of lateral GaN MOSFETs with all-implantation process. The long channel design was used to extract MOS channel characteristics.

3. Results and discussion

AFM images of Mg-implanted GaN surface after high temperature annealing are shown in Fig. 2. The root mean square (rms) roughness calculated by 1 μm square area is 0.18, 0.22, 0.66, and 0.85 nm for as implanted, 1200°C, 1300°C, and 1400°C annealed sample, respectively. The surface roughness increases by increasing annealing temperature, but the AlN cap provides a reasonable surface protection for GaN even for 1400°C resulting an rms surface roughness less than 1 nm.

Fig. 3 shows the I_d-V_g transfer characteristics in the linear region on fabricated GaN MOSFETs. Fabricated MOSFETs show obvious normally-off operation with positive V_{th}. The

V_{th} ~ 10 V is extracted by linear extrapolation of I_d-V_g curve.

The drain current increases with increasing Mg activation annealing temperature, and also V_{th} shows slight increase. The field effect mobility curves calculated from I_d-V_g characteristics are shown in Fig. 4. Corresponding to the drain current increase, the field effect mobility also increases by increasing annealing temperature, and maximum field effect mobility of 48.9 cm2/Vs is obtained on 1400°C annealed sample. Although the surface roughness increases by the high temperature annealing, the MOS channel properties such as field effect mobility and V_{th} don't show deterioration, suggesting that the high temperature annealing contributes the recovery of defects introduced by Mg I/I resulting the improvement of the MOS channel properties. Higher channel mobility would be expected by further increase of activation annealing temperature, but the surface roughness also increases. Because the surface roughness scattering might be concern in those case, it is also necessary to suppress the surface roughening in order to realize higher channel mobility.

3. Conclusions

We have demonstrated the normally-off operation of GaN MOSFET on Mg implanted layers. Although the surface roughness increased by increasing annealing temperature, the Mg activation annealing temperature contributes the improvement of channel characteristics, and we observed the maximum field effect mobility of 48.9 cm2/Vs on the 1400°C annealed sample. The threshold voltage was about 10 V. These results greatly support the realization of vertical MOSFETs with all-implantation process.

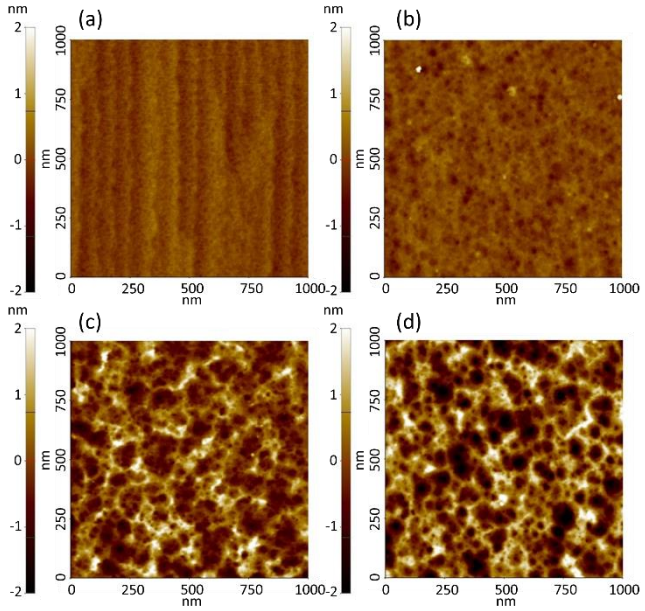

Fig. 2 AFM images of GaN surface. (a) [Mg] = 1×10^{18} cm^{-3} as implanted wafer, (b) after 1200°C annealing, (c) after 1300°C annealing, and (d) after 1400°C annealing.

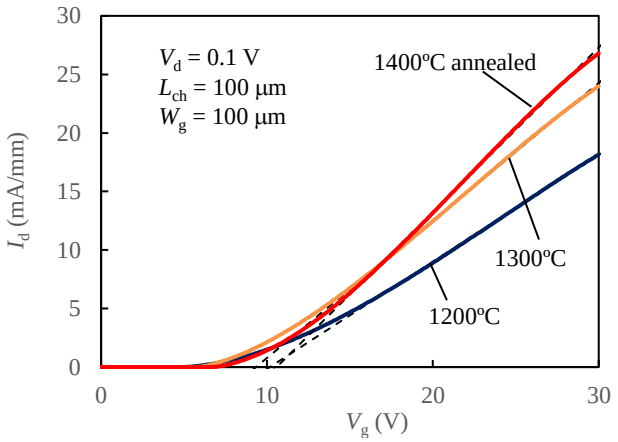

Fig. 3 I_d-V_g transfer characteristics of fabricated GaN MOSFETs with different Mg activation annealing temperature.

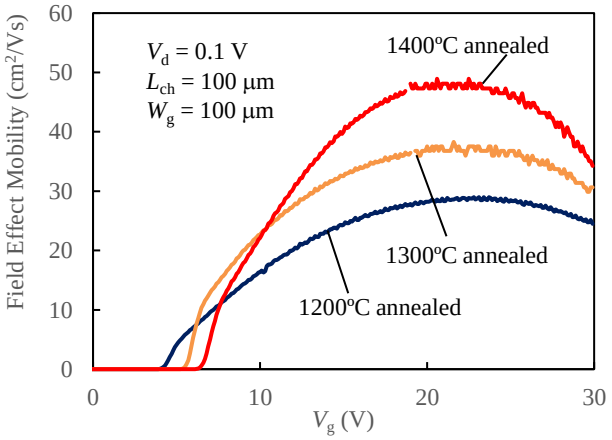

Fig. 4 Field effect mobility curves of fabricated GaN MOSFETs with different Mg activation annealing temperature.

Acknowledgements

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