PS-2-01

Performance of WCN Diffusion Barrier for Cu Through Silicon Vias

Seung Yeon Lee[1,2], Byung Kwon Ju[2] and Yong Tae Kim[1]

[1] Korea Institute of Science & Technology
Semiconductor Materials & Devices Lab.
Seungpook-ku, 14gil 5 Hwaryang-ro, Seoul, Korea
Phone: +82-2-958-5733 E-mail: ytkim@kist.re.kr
[2] Korea Univ.
Display and Nano system Lab., College of Engineering
Seoul 136-713, Korea

Abstract

WCN diffusion barriers has been used for Cu through silicon via (TSV) structure. Comparing with other diffusion barriers, TaN, WN and TiN, Contact resistance of Cu/WCN/Si TSV maintains initial value within 10% deviation at 700℃ annealing since the WCN protects the Cu diffusion. During chemo-mechanical polishing, the WCN offers damage free process.

1. Introduction

Cu through-silicon vias (TSVs) have been studied for 3-dimensional (3-D) integration to provide shorter vertical paths for connection and enable new system architectures. Among challenging issues for Cu TSVs, a continuous diffusion barrier is also important to protect Cu metals from diffusing out from the vias and to keep strong adhesion to withstand chemo-mechanical polishing process [1]. So far, TiN, TaN, WN and RuO, have been popularly used as a diffusion barrier [2-4]. In this work, atomic layer deposited-WCN has been introduced as an alternative diffusion barrier against the Cu diffusion with strong adhesion.

2. Experimental

For the TSV, 150 nm diameter via holes were prepared with high aspect ratio of 20:1 and deposited 20nm WCN thin films with 200 cycles of atomic layer deposition (ALD). Reactant gas system was WF_6-CH_4-NH_3 and the ALD process was operated at a pressure of 0.5 Torr, and 250℃ without plasma enhancement. The reason we didn't use the plasma enhancement system is that good step coverage cannot be expected with the PE-ALD in high aspect ratio via. However, WF_6 is known to generate encroachment and worm hole at the Si surface and the interface of Si/SiO_2. To prevent such defects, we have pre-treated the Si and Si/SiO_2 interface with NH_3 for 20 min, forming the very thin nitride layer. In order to compare diffusion barrier performance, TiN, TaN and WN thin films are also deposited on vias with the same thickness as the WCN and 30-nm-thick Cu seed layers were deposited on these diffusion barriers, preparing Cu/WCN/Si, Cu/TiN/Si, Cu/TaN/Si and Cu/WN/Si cylindrical TSV structures. Contact resistance was measured with these different TSVs. For the 3-D interconnection, we have spin coated 700nm thick methylsilsesquioxane (MSQ) film, as an interlayer dielectric (ILD) material between multi-interconnection. MSQ thin film contains direct Si-CH_3 bonds and has been proved to have excellent crack resistance for the planarization. On these MSQ ILD, diffusion barriers such as TaN, TiN, WN, and WCN are also deposited and thermal stability is tested at higher annealing temperature. Number of damage was investigated with chemo-mechanical polishing (CMP) process since the mechanical strength, surface energy and thermal stability of the Cu/diffusion barrier/ILD/Si structure are closely related with the damascene process of Cu TSVs [5].

3. Results and Discussions

Since the contact resistance usually changes with post annealing process, we have investigated the high temperature reliability of 4 different Cu TSV structures [6]. Cu/TiN/Si, Cu/TaN/Si, Cu/WN/Si and Cu/WCN/Si contact vias are annealed at the temperature of 700℃ for 30 min to accelerate the reliability of the Cu TSVs. Fig. 1 shows the distributions of 100 samples vs the deviation percent of changed resistance/initial one corresponding to 4 different Cu TSV structures. This figure reveals that how many % of TVSs are deviated from the initial resistance after the annealing process at 700℃ for 30 min. 100 % of the Cu/WCN/Si via changes less than 8% deviation range from the initial resistance and

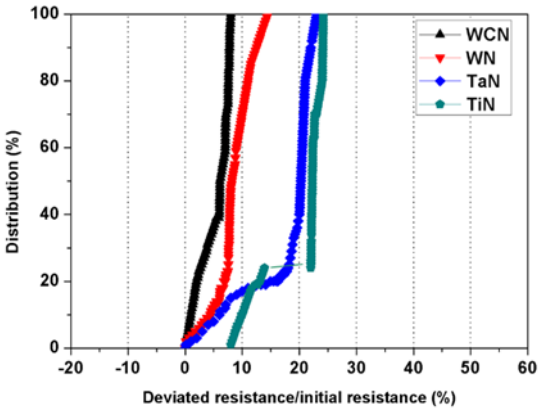

Fig. 1 Distribution of contact resistance vs percent of deviated resistance/initial resistance

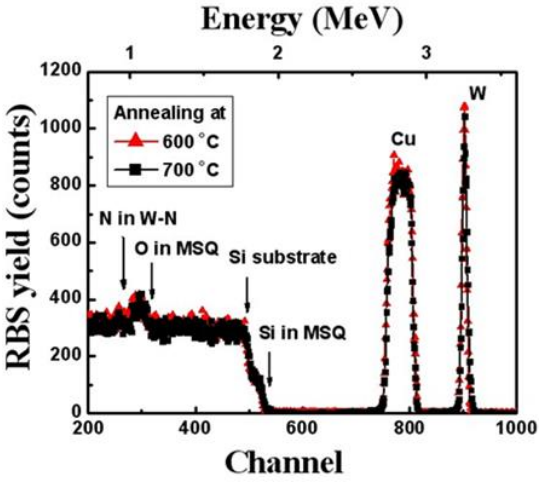

Fig. 2 Rutherford backscattering of Cu/WCN/MSQ/Si structure at the annealing temperatures, 600 and 700 for 30 min

The 80% of the Cu/WN/Si contacts deviates from the initial value by 9~15%. In contrast, 75-80 % of the Cu/TaN/Si and the Cu/TiN/Si contacts swerve from the initial resistance by about 20 %. Serious deviations in the contact resistances of the Cu/TiN/Si and the Cu/TaN/Si vias are due to poor performance of diffusion barriers. It is well known that cu atoms move through grain boundaries more easily than the amorphous barrier films [7]. X ray diffraction and transmission electron microscopy reveal that the TiN is easily formed columnar pillar structure at 5~600℃ and the TaN is also changed into large grains. However, WCN maintains amorphous state till 800℃. The diffusion also creates voids in Cu region and causes contamination in Si to degrade electrical contact. To confirm excellent performance of the WCN diffusion barrier on inter-layer dielectric (ILD), Cu/WCN thin films are deposited on MSQ/Si structures and annealed at 600, 700℃ for 30 min. This contamination causes leakage current of Cu/WCN/ MSQ/Si interconnects due to the Cu diffusion into the Si and ILD layer. Fig. 2 shows Rutherford backscattering spectroscopy (RBS) of the Cu/WCN/MSQ/Si after the annealing processes. In this figure, tail of the Cu peak is obviously separated with Si and W peaks, which means that the WCN barrier successfully prevent the Cu diffusion. However, the Cu/TiN/MSQ/Si and the Cu/TaN/MSQ/Si (RBS data are not shown here) reveal that the Cu peak is partially overlapped with the Ta and Ti peaks and tail of Cu is extended into Si, indicating that the Cu atoms diffuse into the Si region. For the damascene process of Cu TSVs, CMP has been done with 4 different Cu TSVs using slurry and polishing pad and counted the number of damage on accumulative number of wafers [8] as shown in Fig. 3. In this figure, probability number of damage is the biggest in the case of Cu/TiN/Si vias, and second one is the Cu/TaN/Si vias. But, there is nearly no CMP damage on the wafers that have the Cu/WCN/Si vias due to the strong adhesion of WCN.

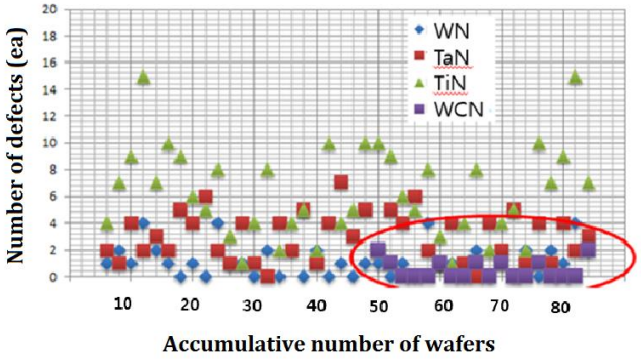

Fig. 3 Number of defects vs accumulative number of wafers corresponding to 4 different Cu TSVs with WN, TaN, TiN, and WCN diffusion barriers

3. Conclusions

ALD-WCN diffusion barriers has been prepared to use for Cu TSVs. Electrical properties of 4 different Cu TSVs, Cu/TiN/Si, Cu/TaN/Si, Cu/WN/Si, and Cu/WCN/Si vias indicate that the WCN has excellent characteristics and maintained stable reliability after the annealing at 700℃ for 30 min because the WCN keeps amorphous state till 800℃. And, the Cu CMP with the WCN barrier guarantees damage free process through 85 accumulative wafers.

Acknowledgements

We would like to express sincere thanks to Samsung Co. and APEX Co. for CMP process and ALD system, respectively. This work is supported by Ministry of Science, ICT and Future Planning under the Grant No. 2U06100 “Extremely low power consumption technology of eDRAM for Internet of Things”.

References

[1] L. Du, T. Shi, P. Chen, L. Su, J. Shen, and G. Liao, Microelectronic Engineering 139 (2015) 31–38

[2] D.J. Kim, J.H. Park, and Y.T. Kim, Jpn. J. Appl. Phys. 40 (2001) 1214.

[3] W. J. Meng, X. D. Zhang, B. Shi, R. C. Tittsworth, L. E. Rehn and P. M. Baldo, Int. Conf. on Metallurgical Coatings and Thin Films, April 22-26, (2002).

[4] .Y.T. Kim and S.I. Kim, Phys. Stat. Sol- Rapid Research Lett, 1 (2007) R47.

[5] S. A. Mior Shahidin and N. A. Fadhil, J. Advanced Review on Scientific Research, 17 (2016) 8-12.

[6] L. Djomeni, Th. Mourier, S. Minoret, S. Fadloun, F. Piallat, S. Burgess, Y. Zhou, and S. Maitrejean, Microelectronic Engineering 120 (2014) 127–132.

[7] Y. Civale, K. Croes, Y. Miyamori, V. Cherman, G. Van der Plas, Zh. Cao, Z. Tokei, E. Beyne, and B. Swinnen, Microelectronic Engineering 106 (2013) 155–159.

[8] Grunlan J. C., Xia X., Rowenhost D, and W. W. Gerberich,, Rev. of Sci. Instr., (2001), 72 (6).