Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp751-752

PS-3-06

Enhancement of Capacitance Benefit by Drain Offset Structure in TFET Circuit Speed Associated with Tunneling Probability Increase

Hidehiro Asai, Takahiro Mori, Takashi Matsukawa, Junichi Hattori, Kazuhiko Endo, Koichi Fukuda
Nanoelectronics Research Institute (Neri), National Institute of Advanced Industrial Science and Technology (AIST)
1-1-1 Umezono, Tsukuba, Ibaraki 305-8568, Japan
Phone: +81-29-861-4160 E-mail: hd-asai@aist.go.jp

The effect of a drain-offset structure on the operation speed of a TFET ring oscillator is investigated by using TCAD simulation. We demonstrate that the reduction of gate-drain capacitance by the drain-offset structure dramatically increases the operation speed of the ring oscillators. Interestingly, we find that this capacitance benefit on the operation speed is enhanced by the increase of the band-to-band tunneling probability. The "synergistic" speed enhancement by the drain-offset structure and the tunneling rate increase will be the promising technology for significant improvement of the operation speed of TFET circuits.

1. Introduction

Tunnel field-effect transistor (TFET) is a one of steep slope transistors that have a gated p-i-n diode structure. The steep switching originating from band-to-band tunneling (BTBT) results in lower *SS* values than 60 mV/dec which is the physical limit of MOSFETs at room temperature [1]. Thus, TFET is expected to be a building block for commercialized logic LSIs in next generation. The integration technology of the TFETs has been developed rapidly. The operation of 23-stage ring oscillator (RO) of Si-based complementary TFET (CTFET) has been demonstrated recently for the first time [2]. To realize practical application of TFET circuits, two main disadvantages of the TFET must be resolved: 1) a large OFF current from the drain edge, and 2) a low ON current. For lowering the OFF current, a drain-offset structure has been proposed [3]. For increasing the ON current, various technologies boosting tunneling rate have been investigated such as isoelectronic trap (IET) technology for Si [4] and channel material engineering with Ge or III-V materials [5]. However, regardless of the progress of such technologies little is known about the effect of the technologies on the operation speed of "TFET circuits".

In this work, we perform mixed-mode TCAD simulations for CTFET ROs and investigate the effect of the drain-offset structure on the operation speed of the ROs. In particular, we investigate the capacitance benefit by the drain-offset structure on the operation speed, and find that the increase of the BTBT rate enhances the capacitance benefit.

2. Model and Method

To analyze the effect of the drain-offset, we considered two types of ROs composed of TFETs w/ and w/o the drain-offset. Figure 1 indicates a schematic figure of the n-type TFET w/ and w/o the drain-offset. For simplicity, we considered minimal 3-stage CTFET ROs. We set input voltage at 1.2V, and the threshold voltage V_{th} of each n/p TFET, which is defined as the voltage where the drain current reaches $|10^{-11}|$ A/μm, is set to ±0.6 V by tuning the gate work function. We performed mixed-mode simulations based on the drift-diffusion approximation by using the device simulator HyENEXSS [6]. The generation rate originating from BTBT, G_{BTBT}, was calculated based on Kane's formula taking account the non-local electric field [7],

$$G_{\mathrm{BTBT}} = A\left(\frac{F}{F_0}\right)^{\gamma} \exp\left(-\frac{B}{F}\right),$$

where $F_0 = 1$ V/cm, F is the non-local electric field. A, B and γ are the material dependent parameters. As described in the above equation, the parameter B dominantly changes the BTBT rate. Hence, in this study, we simulated the tunneling rate increase by simply decreasing the parameter B.

3. Results

Firstly, we chose $A = 2.4\times10^{15}$ cm^{-3}s^{-1}, $B = 1.9$ MV/cm, and $\gamma = 2.5$ and investigate the effect of the drain-offset. Figures 2 (a) and (b) show the drain current I_D and the gate-drain capacitance C_{GD} as functions of the gate-source voltage V_{GS} for n-type TFETs w/ and w/o the drain offset. From Fig. 2 (a), we can clearly see that the OFF current is dramatically reduced by the drain-offset. This is because of the suppression of gate electrostatic control to the tunnel junction at the drain edge. Moreover, as shown in Fig. 2 (b), the drain-offset results in the reduction of the C_{GD} in low V_{GS} region. Note that, even in the presence of the drain-offset, C_{GD} increases in high V_{GS} region where the accumulation layer under the gate connects to the drain. Figure 3 shows the output waveforms of the 3rd stage CTFET of ROs composed of these TFETs. As the figure indicates, the operation speed of the ROs increases by the drain-offset. The drain offset not only suppresses the OFF current, but it also enhances operation speed of the ROs by decreasing the C_{GD}.

Next, we performed similar simulations varying B, and investigate the effect of the tunneling rate increase. Figure 4 (a) shows the I_D of n-type TFETs at 1.2V as a function of B. As B decreases, I_D increases due to the enhancement of tunneling probability. Figure 4 (b) shows the operation frequency of ROs w/ and w/o the drain offset, $f_{w/}$ and $f_{w/o}$, as functions of B. Moreover, in Fig. 4 (c), we show the ratio of $f_{w/}$ and $f_{w/o}$, which is the operation speed enhancement thanks to the C_{GD} reduction, as a function of B. The more ON current increases, the faster the RO operates. This indicates the "speed up" effect thanks to the drain offset is reinforced by the tunneling rate increase. The unique dependence of the C_{GD} on the gate voltage explains this phenomenon. Figure 5 shows the C_{GD}-V_{GS} and I_D-V_{GS} curves of n-TFET w/ the drain offset for B = 1.1, 1.5 and 1.9 MV/cm, respectively. As can

be seen from this figure, V_{th} changes with B even though the onset voltage of C_{GD} corresponding to the carrier accumulation under the gate does not change. Unlike MOSFETs, the current onset of TFETs does not depend on the carrier generation under the gate, and V_{th} is irrelevant to the onset voltage of the capacitance. Therefore, by decreasing B, V_{th} becomes much smaller compared to the onset voltage of C_{GD}, and the C_{GD} benefit by the drain offset is emphasized.

4. Conclusion

In this work, we have investigated the correlation between the capacitance benefit by the drain-offset structure and tunneling rate increase on the operation speed of TFET ROs by using mixed-mode TCAD simulations. We found that the both technologies synergistically speed up the operation of the ROs. This is because of the unique relationship between V_{th} and C_{GD} in TFETs, that is, the decrease of V_{th} of TFETs by the tunneling rate increase is independent of the formation of the accumulation layer.

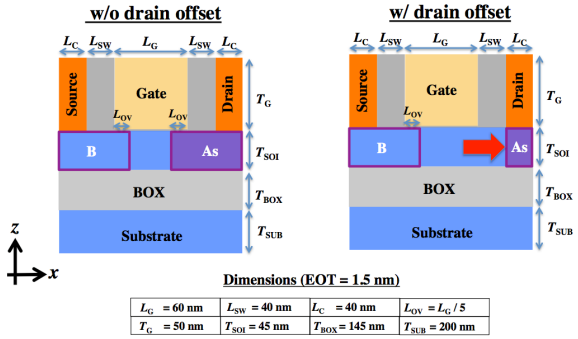

Fig. 1. Schematic figure of the n-type TFET w/ (Left) and w/o (Right) the drain-offset.

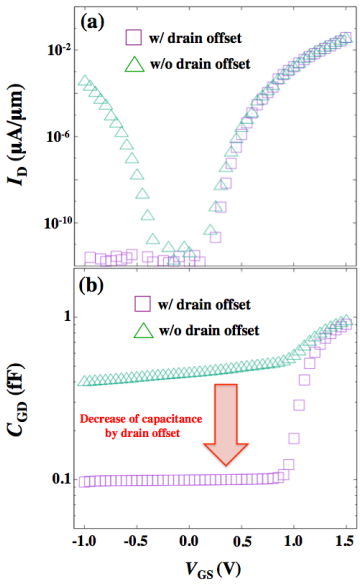

Fig. 2. (a) I_D-V_{GS} curves and (b) C_{GD}-V_{GS} curves of n-type TFETs w/ and w/o the drain offset.

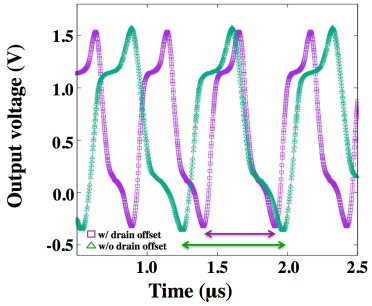

Fig. 3. Output waveforms of the 3rd stage CTFET of ROs w/ and w/o the drain offset.

Acknowledgement

This paper is partially based on results obtained from a project commissioned by the New Energy and Industrial Technology Development Organization (NEDO).

References

[1] W. Y. Cho *et al.*, IEEE Electron Device Lett. **28,** 743 (2007)

[2] T. Mori *et al.*, IEDM Tech. Dig. 512 (2016)

[3] A. Verhulst *et al.*, APL 91, 053102 (2007).

[4] T. Mori *et al.*, APL 106, 083501 (2015).

[5] S. Takagi *et al.*, Symp. VLSI Technol. Dig. Tech. Papers, 22-23 (2015).

[6] HyENEXSS, ver.5.5.7

[7] K. Fukuda *et al.*, Proc. Int. Workshop Comput. Electoron p. 206 (2014).

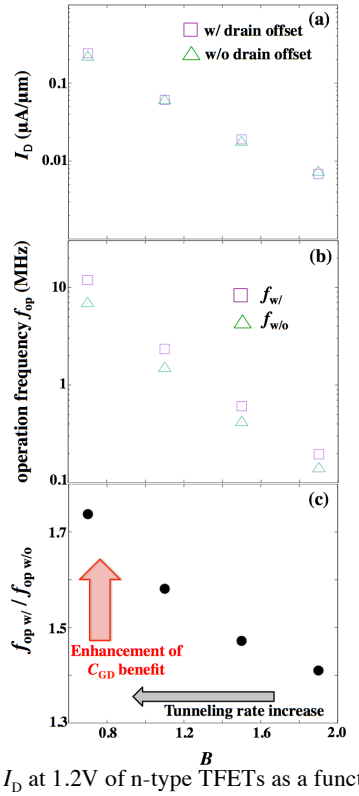

Fig. 4. (a) I_D at 1.2V of n-type TFETs as a function of B. (b) Operation frequency of ROs w/ and w/o the drain offset, $f_{w/}$ and $f_{w/o}$, as functions of B. (c) Ratio of $f_{w/}$ to $f_{w/o}$ as a function of B.

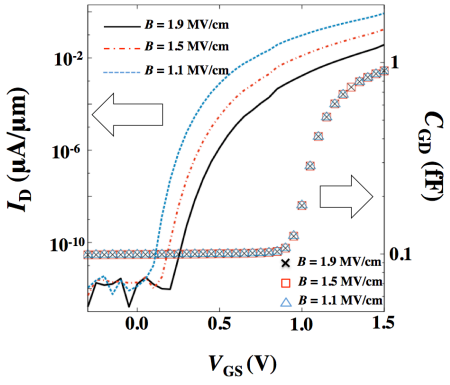

Fig. 5. I_D-V_{GS} and C_{GD}-V_{GS} curves of n-type TFETs w/ the drain offset for B = 1.1, 1.5 and 1.9 MV/cm.