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Benchmarking the Impact of Work Function Variations on Cell Stability of Low-Voltage 6T SRAMs with Non-planar and Planar TMDFETs

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***Abstract* — This work benchmarks the impacts of work function variations (WFV) on the cell stability of low-voltage SRAMs with non-planar and planar transition-metal-dichalcogenide (TMD) FETs based on ITRS 2028 (5.9 nm node) with the aid of atomistic TCAD mixed-mode simulations. Our study indicates that, with the same ON-current and similar foot print size in 6T SRAM, the non-planar TMD structure exhibits better immunity to WFV and larger read static noise margin (RSNM). Besides, the source/drain resistance, a major concern of TMD devices, may not be an issue for the cell stability of low-voltage SRAMs.**

Introduction

With atomically-thin channel thickness and adequate band-gap, 2D transition-metal-dichalcogenide (TMD) devices such as MoS_2 and WSe_2 FETs [1], [2] are attractive candidates for future extremely scaled low-voltage SRAMs.

For the extremely scaled transistors, the impact of random variations such as work function variation (WFV) [3] on the cell stability of SRAMs is a big challenge, especially for low-voltage SRAMs. Compared with planar TMD devices, non-planar TMD devices [4], [5] can provide higher drive current under the same foot print because of their FinFET-like structure. However, how might the non-planar TMD structure affect the immunity to WFV has rarely been known and merits investigation.

In this work, we benchmark the impacts of WFV on the cell stability of 6T SRAM with planar and non-planar TMD devices. The influence of source/drain resistance (R_{SD}) will also be evaluated.

Device Design and TCAD Simulation Methodology

Monolayer and bilayer MoS_2-n/WSe_2-p devices are considered for planar and non-planar structures (Fig. 1). The pertinent device parameters (Table I) for planar structure are based on the ITRS 2028 (5.9nm node) [6] spec. The critical dimensions of non-planar devices are chosen to have similar foot print of SRAM cells to the planar one. The devices are designed with equal ON-current. Fig. 2 shows the I_{DS}-V_{GS} curves of the four kinds of devices. Source/drain series resistance of 128 Ω-μm is adopted based on the ITRS 2028 spec. The mobility of four kinds of devices are based on [7]. To assess the WFV, the Voronoi TCAD atomistic simulation methodology [8] is carried out with grain size = 4.3nm and 2nm, respectively.

Results and Discussions

Fig. 3 demonstrates the layouts of 6T SRAM cells with planar and non-planar TMD devices. These two cells possess almost the same area. Fig. 4 compares the nominal RSNM of the four different MoS_2-n/WSe_2-p 6T SRAM cells at V_{DD}= 0.4V. Non-planar monolayer SRAM exhibits the highest RSNM due to its better device electrostatics and higher threshold voltage.

Fig. 5 shows that, with grain size =4.3nm, the non-planar monolayer SRAM has the best RSNM μ/σ ratio. Notice that the RSNM μ/σ ratio of all the four types of cells fail to meet the 6σ requirement,and the SRAM cell with non-planar devices possesses better RSNM μ/σ ratio mainly due to their lower σRSNM. In order words, taking advantage of the third dimension to increase the gate area under the same footprint, the non-planar TMD can possess better immunity to WFV.

Fig. 6 indicates that with grain size reduced to 2nm, the RSNM μ/σ ratio of the SRAM cells with non-planar monolayer/bilayer devices can potentially meet the 6σ requirement. However, for SRAM cells using planar devices (Fig. 6(b)), some read-assist circuit techniques such as bootstrapped dynamic power rails [9] or the standard 8T cell are necessary to have better μ/σ ratio.

R_{SD} has been recognized as one of the critical performance limiting factors for TMD devices [10]. The impacts of R_{SD} on the RSNM variability under super-threshold (V_{DD}= 0.64V) and near-threshold (V_{DD}= 0.4V) operation are shown in Fig. 7, respectively. It can be seen that for both grain sizes (4.3nm and 2nm), the RSNM μ/σ ratio o f all the SRAM cells at V_{DD} = 0.64V decreases with considering R_{SD}, while at V_{DD} = 0.4V the impact of R_{SD} is negligible. In other words, the R_{SD} may not be a stability concern for low-voltage TMD-based SRAM cells.

Acknowledgement

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Reference

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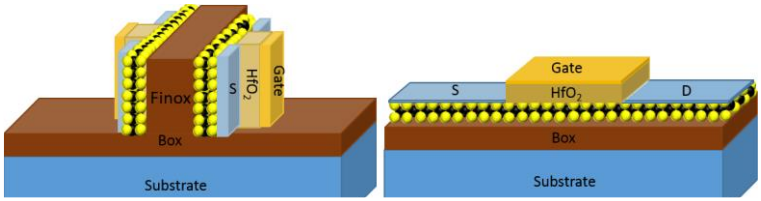

Fig. 1. (a) Schematic of a non-planar TMD device where a thin film of TMD is grown in a conformal way around SiO_2 etched fin [4]. (b) Schematic of a planar TMD device.

Table I. Device parameters used in this work

Planar		Non-planar	
L_g [nm]	5.9nm	L_g [nm]	5.9nm
W[nm]	5.9nm	H_{fin} [nm]	12nm
T_{ch}[nm]	0.65nm	W_{finox}[nm]	1nm
EOT[nm]	0.41nm	EOT[nm]	0.41nm
T_{box}[nm]	10nm	T_{box}[nm]	10nm

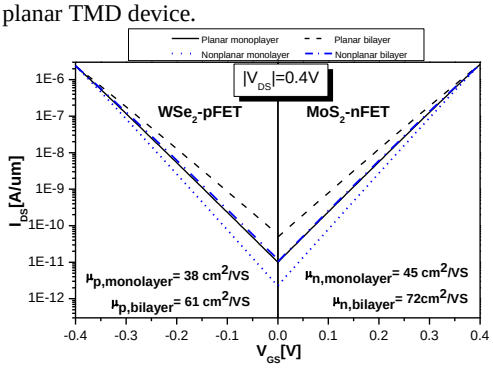

Fig. 2. I_{DS}-V_{GS} curves of MoS_2-n and WSe_2-p devices with equal I_{on}.

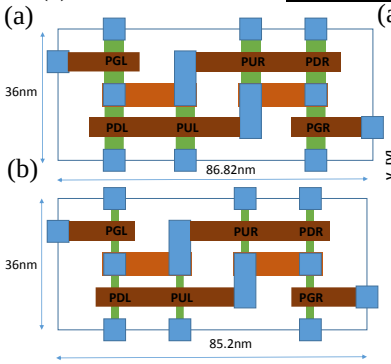

Fig. 3. SRAM layouts with (a) planar and (b) non-planar TMDFETs.

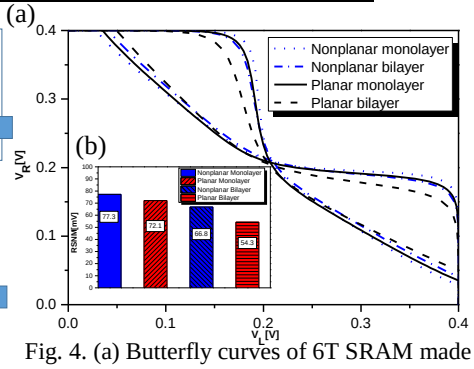

Fig. 4. (a) Butterfly curves of 6T SRAM made of four TMDFETs. (b) Comparison of RSNM value at V_{DD}=0.4V

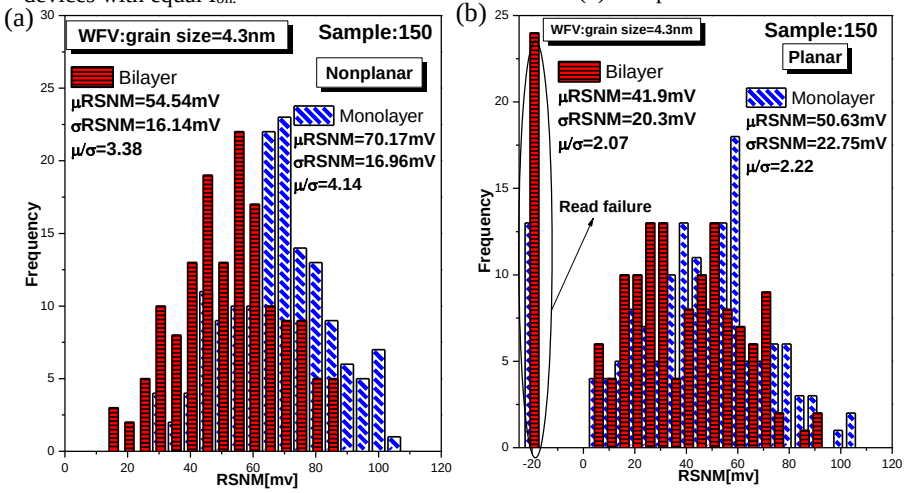

Fig. 5. RSNM variability comparisons for (a) non-planar and (b) planar MoS_2-n/ WSe_2-p 6T SRAM cells considering WFV at V_{DD} = 0.4V with grain size = 4.3nm

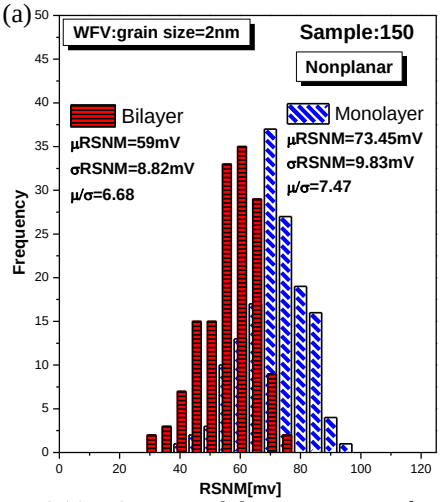

Fig. 6 (a). RSNM variability comparisons for non-planar 6T SRAM Cells considering WFV at V_{DD}=0.4V with grain size =2nm

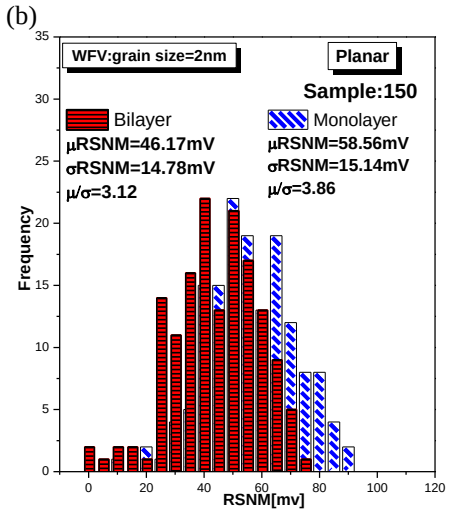

Fig. 6 (b). RSNM variability comparisons for planar 6T SRAM Cells considering WFV at V_{DD}=0.4V with grain size =2nm

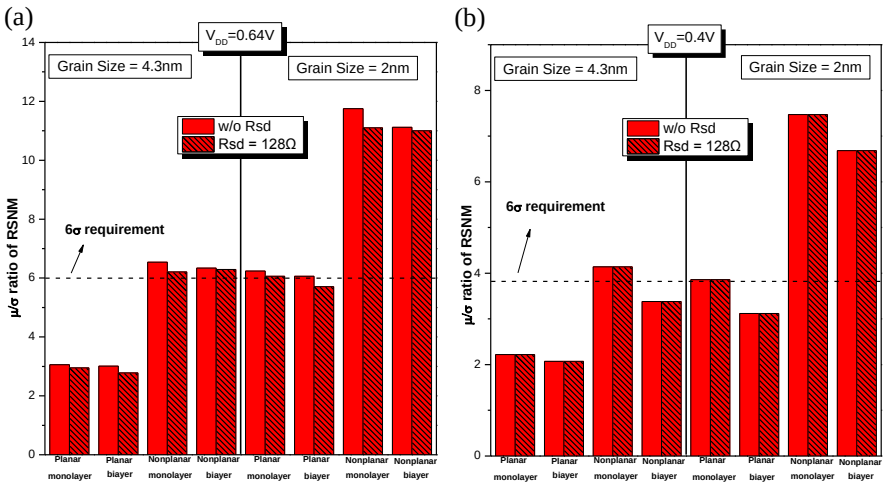

Fig. 7 Impacts of R_{SD} on the RSNM variability of 6T SRAM cells at (a)V_{DD} = 0.64V and (b) V_{DD} = 0.4V with grain size =4.3nm and 2nm.