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Numerical Design for Power Integrity Analysis of Tunnel Field Effect Transistors

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Abstract

In this paper, a thermal behavior of tunnel FETs is presented for the first time. Thermal analysis based on mask layout data, namely Graphic Data System (GDS) of TFETs circuit is carried out using Silvaco InVar™. Here, we compare the thermal behavior of TFETs with that of low-power CMOS. It is shown that the chip surface temperature of TFETs circuit does not change from an environmental temperature due to the smaller on-current of TFETs than that of low power CMOS.

1. Introduction

Tunnel field effect transistors (TFETs) are promising device structures [1,2,3] for an ultra-low power circuits application especially used for battery based computing like IoT devices. In spite of the advantage of the steep subthreshold slope, the small tunneling efficiency between source and channel in a Si band-gap results in low on-current (I_{on}), as shown in Fig 1 (a). It is believed that low frequency operation ranges of MHz to kHz are suitable to TFETs [4] and the power consumptions of TFETs are smaller than that of conventional CMOS. Fig 1 (b) and (c) show the circuit simulation results using SmartSpice™ [5] for ring oscillator (RO) with TFETs and 65nm CMOS, respectively. It is found that an active power of TFETs is smaller than that of CMOS, because TFETs have slow operating speed. However, the heat generation during operation will not be negligible, when the circuit area composed of TFETs is small compared to the area of thermal diffusion defined by the thermal rate of chip layers. In this study, we compare the thermal behavior of TFETs with that of low-power CMOS listed in Table I. TFETs are ideal version of experimentally fabricated one [3]. In order to clarify the advantage of low-power operation of TFETs also from the viewpoint of the heat generation, 3D quantitatively investigation using Silvaco InVar™ [5] is performed.

2. Simulation methods

Analysis of power integrity has been a significant bottleneck in the physical verification of transistor level designs, because the need for accurate and increasingly complex analysis to be performed on designs ranging from single block to full-chip. We use GDS file of 101-stages RO and layer map for the input data of InVar™ thermal analysis. Figure 2 (a) shows the circuit diagram of RO with TFETs, which includes inverter and output buffer as shown in Fig. 2 (b). Thermal conductivity and diffusivity are listed in Table II and the layout of input block on virtual chip with 3[mm] square is shown in Fig. 3. Figure 4 shows the cross sectional view of chip-layers. Interconnect layers up to M3 layer are considered and total layer thickness is 2μm. Here, the environmental temperature (T_{env}) is 27°C through thermal resistivity of package (R_θ) with 100°C/W. In this study, a total power (P_{tot}) of each circuit on input block was estimated from the peak current of operated transistors and the operation voltage (V_{dd}).

3. Simulation Results

3-1. Thermal behavior of low-power CMOS for V_{dd}=1.5V

Figure 4 (a) shows the temperature gradients on the chip surface with low-power CMOS of V_{dd}=1.5V listed table 1, where gradual heat distribution with an average temperature of 64.32°C was presented. Local heat generation over 70°C around the NFETs with large I_{on} of output buffer and PFETs near the voltage source of inverter was observed, as shown in Fig. 4 (b). It is found that chip surface temperatures tend to increase as the current flow increase and a hot spot generates when the transistor had a large operating current, even though the smaller area of circuit.

3-2. V_{dd} dependence on the thermal behavior

Low power aspects, the small operating current as well as low V_{dd} is most efficient As shown in Fig. 5, due to the smaller current of TFETs especially in low V_{dd} regime, P_{tot} of TFETs is 3-ordered of magnitude smaller than that of low-power CMOS, which is consistent with the circuit simulation results of Fig. 1 (b) and (c). Figure 6 shows the chip surface temperature for both low-power CMOS and TFETs, where the theoretical values defined by ($R_\theta . P_{tot} + T_{env}$) were good agreement with the extracted average temperature (Fig. 6 (a)). The maximum temperatures were proportional to the temperature of a hot spot with the high operating current of transistors. Comparing TFETs with low-power CMOS, it is found that the chip surface temperature of TFETs does not change from T_{env} in order to the low I_{on}. Furthermore, the thermal behavior of TFETs was independent of V_{dd} with 0.3 to 1.2V. It is suggested that the heat generation of TFETs circuit rarely happened in whole operating regime.

4. Conclusions

3D analysis of thermal behavior was presented for the first time. GDS based analysis of TFETs was carried out using Silvaco InVar™. It was found that the chip surface temperature of TFETs circuit does not change from T_{env} due to the smaller I_{on} of TFETs than that of low power CMOS. These results suggest that TFETs are promising candidate for the circuits with small heat generation even in low power operation like IoT devices.

Acknowledgements

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References

[1] C. Hu, *et al*., IEDM Tech. Dig. (2010) 387. [2] K. Jeon, *et al*, VLSI Symp., (2010) 121. [3] Y. Kondo, *et al*, SSDM 2013, (2013). [4] T. Tanamoto, *et al*., SSDM 2017 to be submitted. [5] Silvaco, [online] http://www.silvaco.com/ [6] R. Fox, *et al*., IEDM (2005), S. Hasegawa, *et al*., IEDM (2008), C.-H. Jan, *et al*., IEDM (2012).

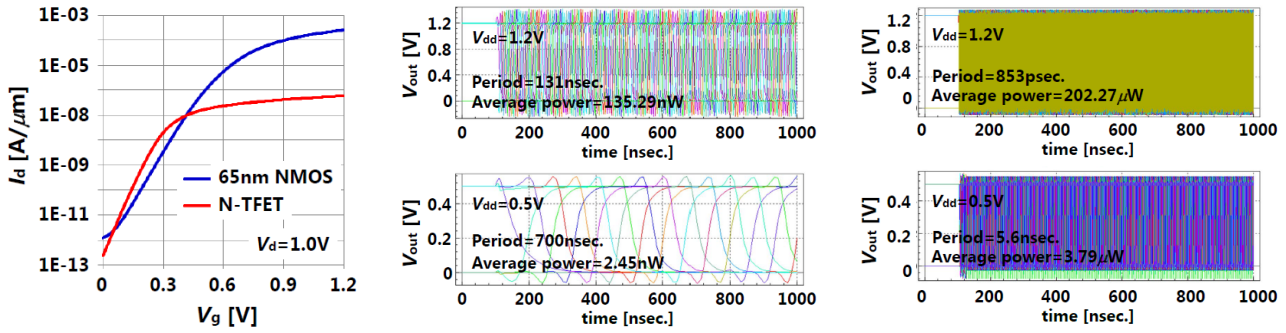


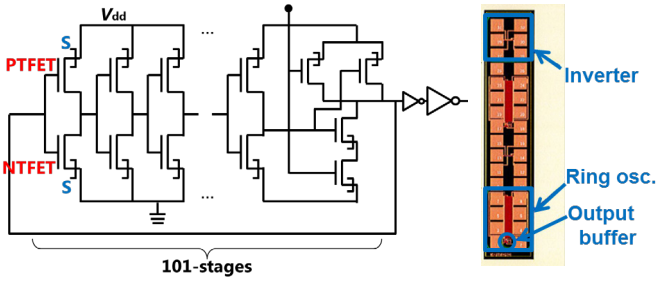
Fig. 2 (a) I_d-V_g characteristics of N-TFET and 65nm NMOS. (b) and (c) show the circuit simulation results with V_{dd}=1.2V and 0.5V for TFETs and 65nm CMOS RO, respectively. The period and active power show in each graph.

Table I Targeted I_{on} of both TFETs and low-power CMOS [6]

V_{dd} [V]		1.5	1.3	1.2	1.1	1	0.8	0.5	0.
I_{on} [A/μm]	LP NMOS	7.50E-04	5.04E-04	5.19E-04	6.66E-04	6.84E-04	7.28E-04		
	LP PMOS	3.50E-04	2.35E-04	2.66E-04	3.33E-04	3.42E-04	3.64E-04		
	NTFET				1.48E-06	1.09E-06	6.97E-07	7.16E-08	2.10E-0
	PTFET				1.06E-06	7.58E-07	5.00E-07	4.62E-08	1.36E-0

Table II Thermal parameters

Layer	Thermal conductivity [W/(m°C)]	Thermal diffusivity [m²/sec]
Substrate	168	8.8E-05
Insulator	1.38	8.3E-07
Interconnect Layer 1 (M1)	168	8.8E-05
Interconnect Layer 2 (M2)	401	1.11E-04
Interconnect Layer 3 (M3)	205	9.7E-05



(a) (b)

Fig. 2 (a) Circuit diagram view of 101-stages RO with F/O=3 using TFETs. (b) Overall view of input block, which includes inverter, ring oscillator and output buffer.

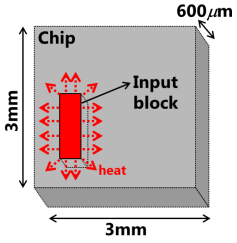


Fig. 3 Layout of input block on virtual chip with 3mm square and the direction of heat diffusion.

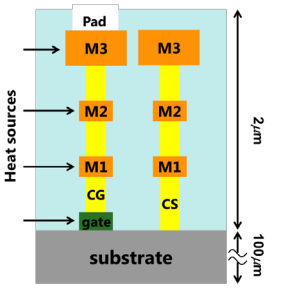


Fig. 4 Cross sectional view of chip-layers of input block connected to the environmental through the thermal resistance of package.

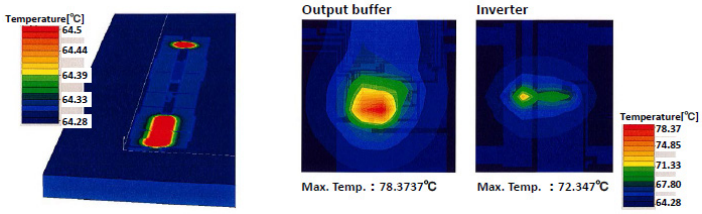


Fig. 4 Temperature gradients on the chip surface with low-power CMOS at V_{dd}=1.5V. (a) Gradual heat distribution with an average temperature of 64.32°C is presented. (b) Hot spot located in output buffer and inverter.

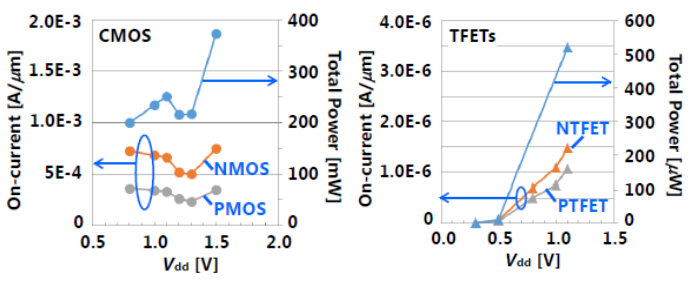


Fig. 5 V_{dd} dependence of I_{on} and P_{tot} for (a) low power CMOS and (b) TFETs.

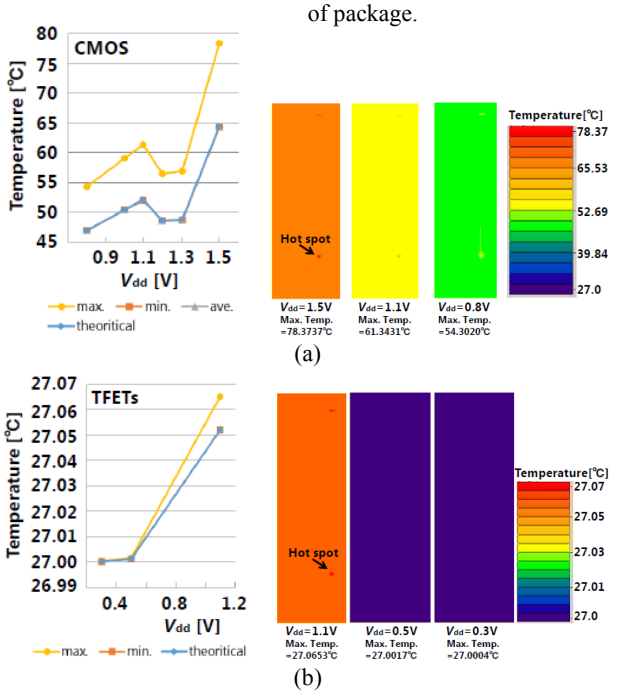


Fig. 6 V_{dd} dependence on chip surface temperature for (a) low power CMOS and (b) TFETs, where the theoretical values defined by (R_θ . P_{tot} + T_{env}).